TECHNICAL MANUAL

OPERATION INSTRUCTIONS
MAINTENANCE INSTRUCTIONS
WITH PARTS LIST

DIGITAL MULTIMETER
PART NUMBER, 3102494-003

GENERAL DYNAMICS ELECTRONICS

Contract Number: F41608-82-C-0110

Racal Dana

MODEL 5005-S

SHORT CHG 1.

PUBLISHED UNDER AUTHORITY OF THE SECRETARY OF THE AIR FORCE

MARCH 1984

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GLOSSARY

Abbreviations

A/D	Analog-to-Digital
AH1	Acceptor Handshake
ATN	Attention
AZ	Auto Zero
CO	Controller
CR	Carriage Return
DAV	Data Valid
DCL	Device Clear
DMM	Digital Multimeter (Racal Dana)
DT1	Device Trigger
EOI	End or Identify
E1	Open Collector Bus Drivers
FET	Field Effect Transistor
GET	Group Execute Trigger
GPIB	General Purpose Interface Bus (IEEE-488-1978)
GTL	Go To Local
IFC	Interface Clear
IRQ	Interrupt Request
LEO	Extended Listener
LF	Line Feed
LLO	Local Lock Out
L4	Listener

Abbreviations

M/Z	Measure Zero
NDAC	Not Data Accepted
NMI	Non-Maskable Interrupt
NRFD	Not Ready For Data
NVM	Non-Volatile Memory
OC	Opto Couplers
PPO	Parallel Poll
QF	Quantized Feedback
RAM	Random Access Memory
REN	Remote Enable
RL1	Remote/Local
ROM	Read Only Memory
SDC	Selected Device Clear
SH1	Source Handshake
SPD	Serial Poll Data/Disable
SPE	Serial Poll Enable
SRQ	Service Request
SR1	Service Request
TEO	Extended Talker
T5	Talker
U/D	Up Down
UNL	(Unlisten) bus message
μP	Microprocessor
UNT	Untalk

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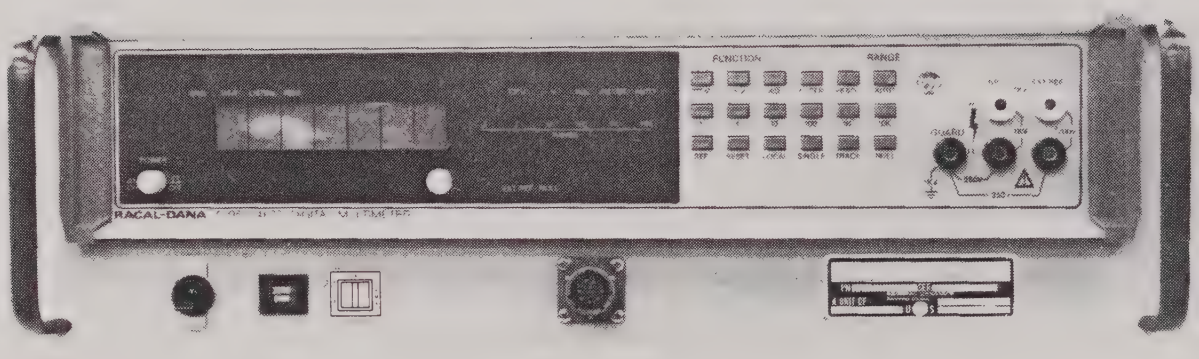

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Figure 1-0. Digital Multimeter Assembly 3102494-003

SECTION 1

GENERAL DESCRIPTION

1-1. PURPOSE. This Instruction Manual supplies the operation procedures essential in optimizing the capabilities designed into the instrument, also, the Instruction Manual details the calibration and maintenance procedures required by technical personnel. These service procedures are necessary to obtain the maximum performance specified. It is recommended that the users and technicians read this manual before operating the instrument.

1-2. SCOPE. The scope of this manual includes installation, operation, and maintenance guidelines pertinent to the instrument. The following subsections are included to support operation and maintenance activities: Installation, Operation, Theory of Operation, Maintenance, Drawings and Parts List.

1-3. DESCRIPTION. The Digital Multimeter Assembly contains two modules; the Racal-Dana Model 5005-S-4622 Digital Multimeter and the General Dynamics Electronic Division Interface Assembly 3102494.

The Racal-Dana Digital Multimeter (DMM) is fully described in the appropriate section of this manual. The analog signal and reference inputs are available on both the front and rear panels of the DMM. The terminals on the rear are connected through the interface to the input from the test station. Manual control of the instrument is from pushbuttons on the front panel. Remote control of the instrument is by means of the IEEE-488 bus connector on the rear of the instrument. All instrument automatic functions are controllable through this bus and are fully described in Section 3 Theory of Operation.

The interface assembly contains the Racal-Dana DMM and provides the same exterior dimensions and mounting locations as the CIMRON E9500B-991B that it replaces in the F-111 test stations.

1-4. ELECTRICAL DESCRIPTION.

1-5. Interface Electrical. The interface assembly contains a microprocessor based controller to convert signals to and from the test station to the required IEEE-488 bus in the Racal-Dana DMM. Signals from the test station are isolated using optical isolators. A block diagram of the DMM and interface is shown in figure 1-1.

1-6. DMM Electrical Description. The Racal-Dana Model 5005 microprocessor (μP) based digital multimeter (DMM) is a 5-1/2 digit auto-ranging multimeter. The basic functions include 5 DC volt scales ranging from 0.1 volt to 1 KV; 4 AC volt scales ranging from 1 volt to 1 KV, and 6 resistance measurement scales ranging from 0.1K ohm to 10,000K ohms. The chart in table 1-1 represents the DMM function and ranges. For systems applications, the Model 5005 features an IEEE-488-1978 (GPIB) interface.

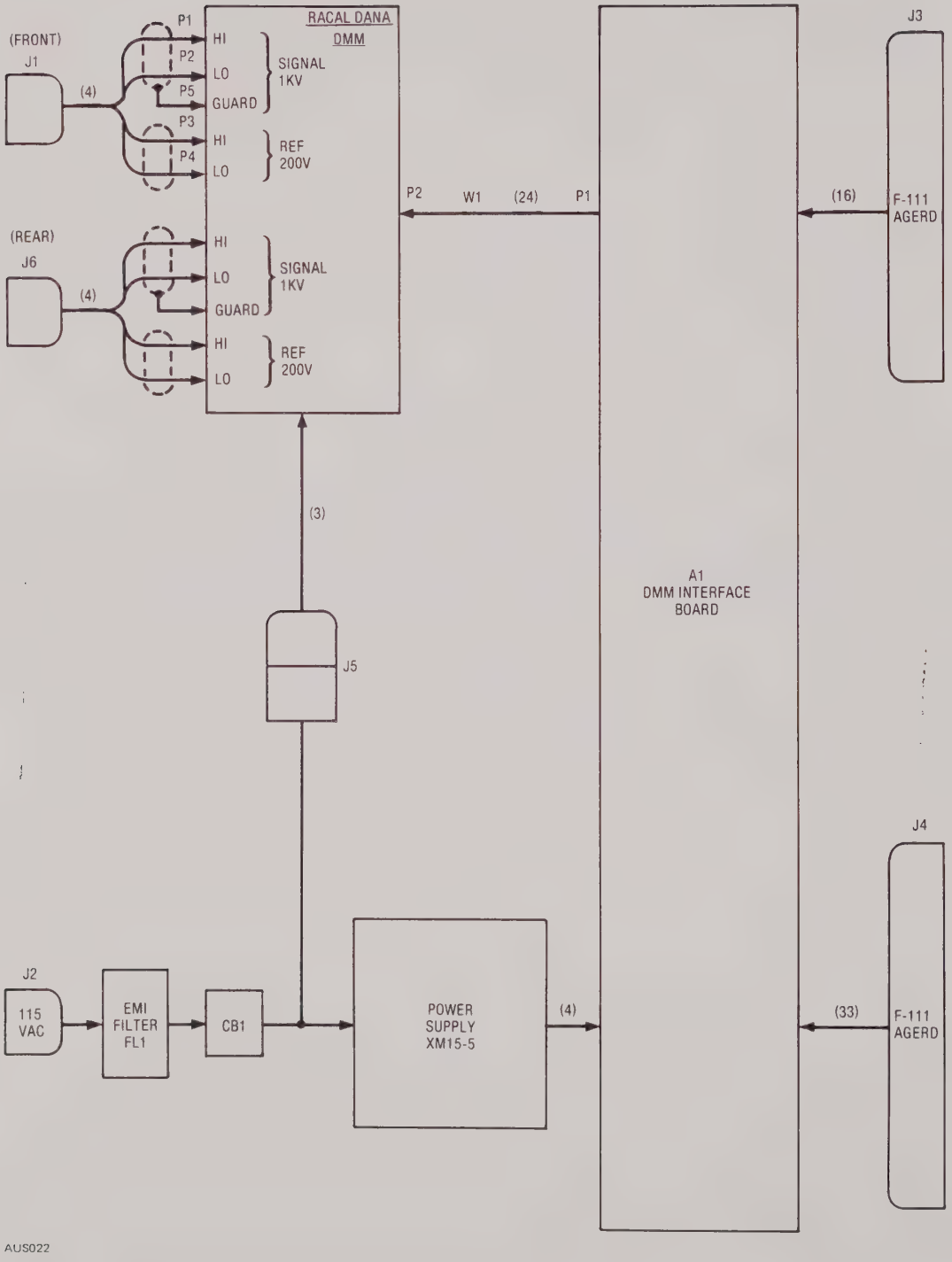

Figure 1-1. DMM and Interface Block Diagram

Table 1-1. DMM Function and Range

RANGE	FUNCTION		
	DC	AC	OHMS
0.1V	X		
1V	X	X	
10V	X	X	
100V	X	X	
1000V	X	X	
.1K			X
1K			X
10K			X
100K			X
1000K			X
10000K			X

The DMM measurement process depicted in the block diagram figure 1-2 consists of three major parts:

a. The Signal Conditioning section where the input signal is switched, scaled, attenuated, rectified, and filtered to 2 VDC full scale.

b. The Analog-to-Digital converter employs a Quantized Feedback conversion technique, to change the DC voltage into a representative digital signal.

c. The microprocessor-based digital section translates the analog-to-digital (A/D) converter output to a numerical value on the instrument display that represents the value of the input signal. The digital section also provides range control, decimal placement and programming.

1-7. MECHANICAL DESCRIPTION. The physical configuration of the DMM assembly is outlined in figure 1-3. The front panel contains the main power ON-OFF switch (circuit breaker), ZERO OHM pushbutton, REBAL pushbutton, and connector J6 used for ratio measurement. The rear panel contains connector J1 that interfaces with the Racal-Dana DMM through cable W1, connectors J3 and J4 that interface with the F-111 test station, and connector J2 power input connector. The DMM interface configuration is outlined in figure 1-4, a dimensional outline projecting the front and rear views from the top elevation. The front panel contains the keyboard switches, the LED display, signal input terminals, and reference input terminals. The rear panel contains signal input terminals, reference input terminals, 24 pin GPIB connector, GPIB address switch, two BNC connectors, 3 prong AC power plug and fuse.

1-8. POWER REQUIREMENTS. The DMM and interface is designed to operate from 115 volt AC 10%, at 60 Hz. The interface contains a Xentek XM15 dual DC power supply with separate outputs of 5 volt DC, 1.5 amps. The Racal-Dana DMM may be removed and operated as a separate unit. It is designed to operate from a wide range of AC line voltages and frequencies with 120 VAC and 60 Hz considered standard. The selectable multi-tapped primary winding will accommodate line voltages of 100, 120, 220, and 240 VAC 10%, 47 to 440 Hz. A multi-tapped secondary with four separate windings develop the low voltage supplies required to power the DMM circuits. The installation section presents the AC line cord requirements. The detail power supply circuits are covered in the Theory of Operation section.

1-9. SPECIFICATIONS. The published specifications for the Racal-Dana Model 5005 are listed in table 1-2. These specifications establish the validation for the calibration and specification checks listed in this manual.

1-10. TOOLS AND TEST EQUIPMENT. Tools and test equipment required for maintenance and calibration of the Racal-Dana DMM 5005 are listed in table 1-3.

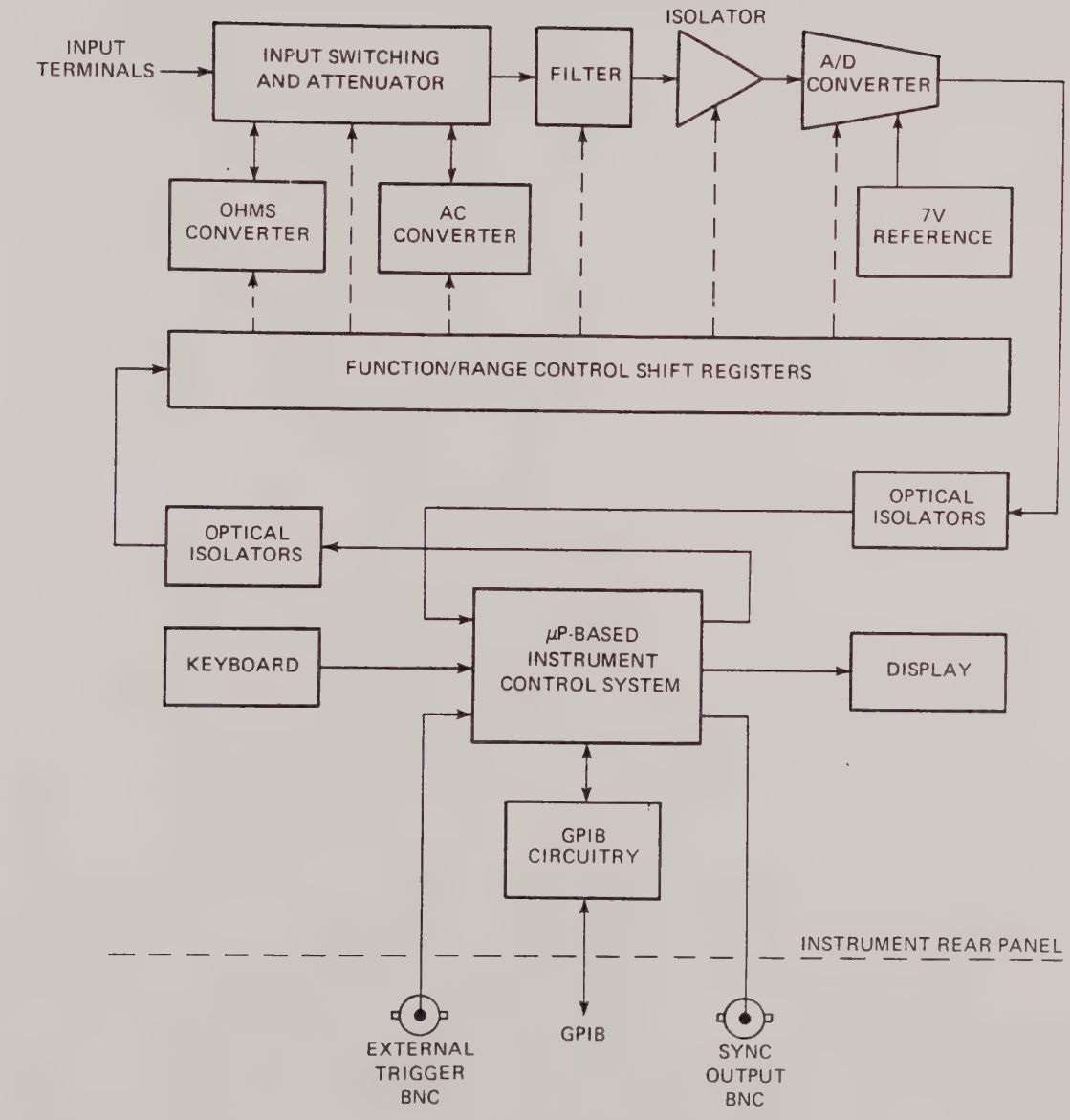

Figure 1-2. Model 5005 DMM Block Diagram

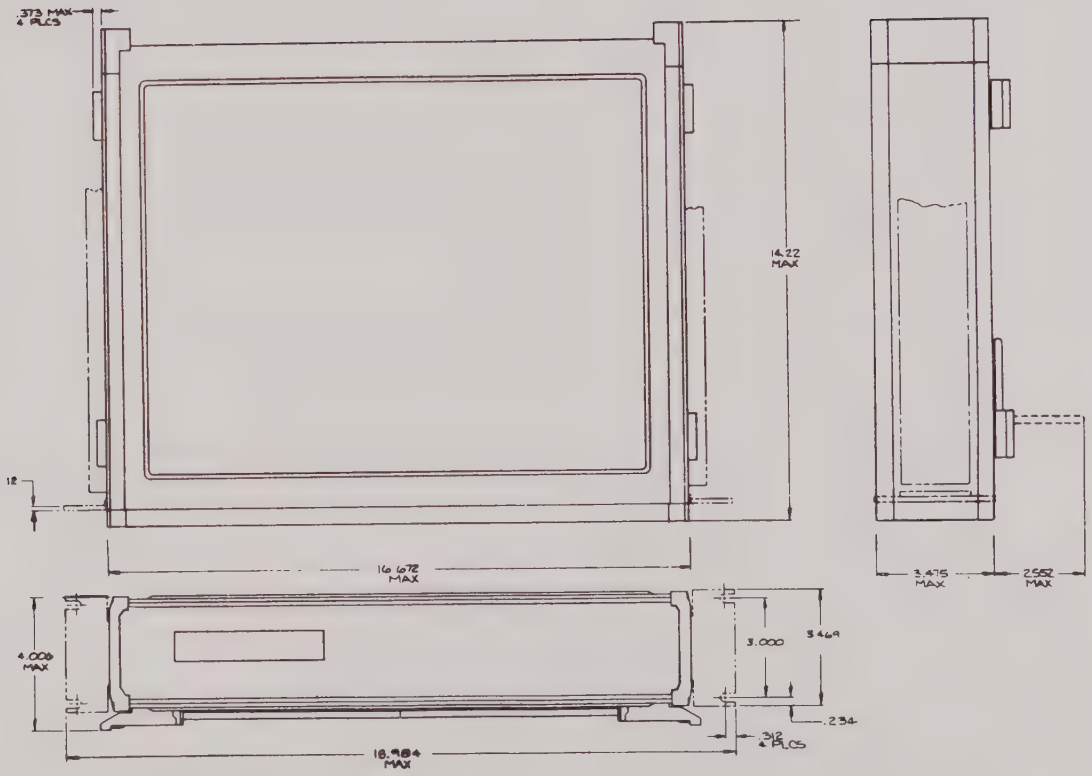

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Figure 1-3. DMM Dimensional Outline

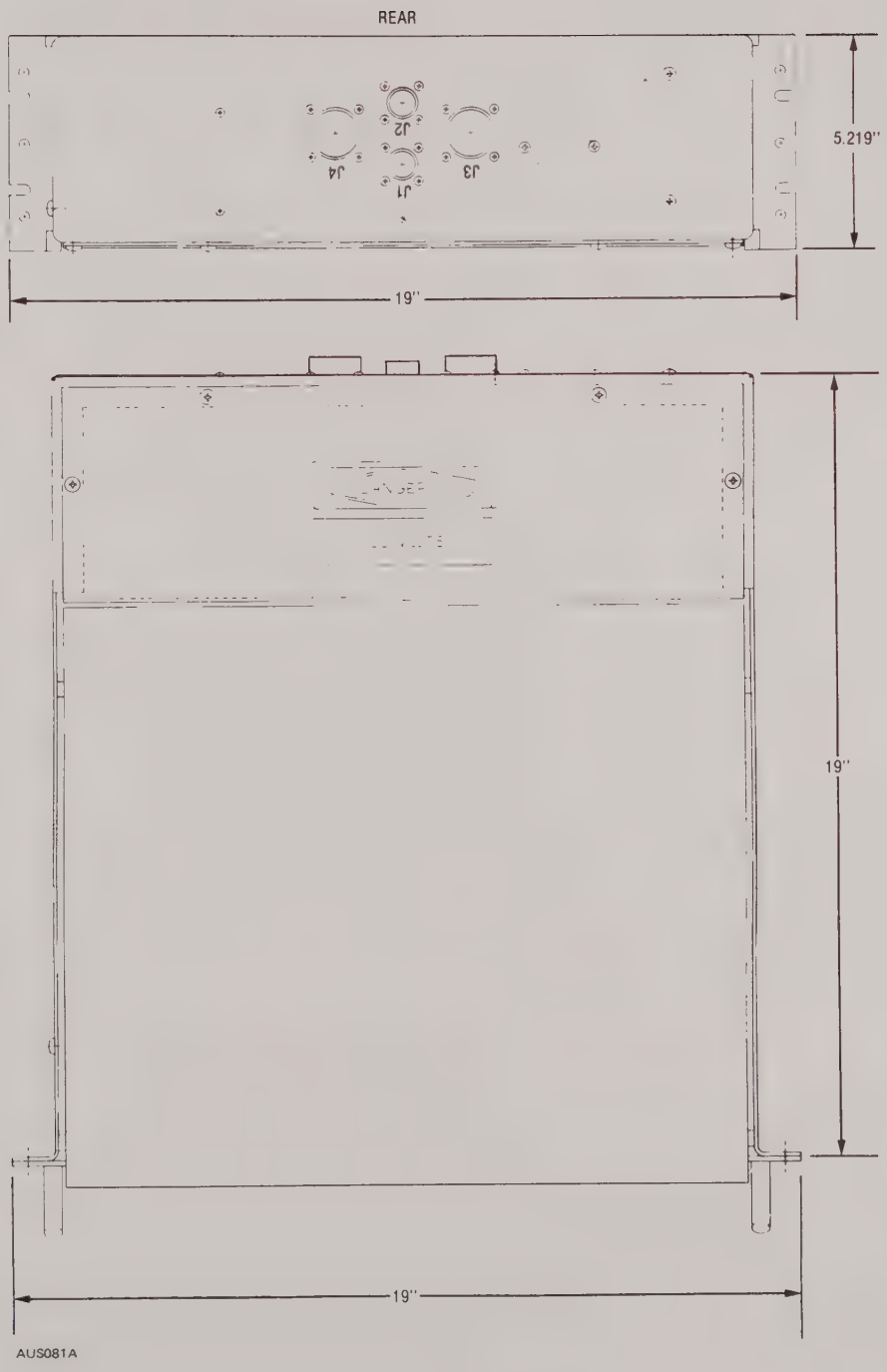

Figure 1-4. DMM Interface Dimensional Outline

Table 1-2. Performance Characteristics

PARAMETER	SPECIFICATION
OPERATING VOLTAGE	115 volt AC ±10%, 60 Hz
DC VOLTS (Interface Power Supply - dual output)	(A) 5V, 1.5A (B) 5V, 1.5A
DC VOLTS (DMM) Ranges	.2, 2, 20, 200, 1000 volts
Accuracy After zero on .1V 24 hr., 23° ± 1°C	.2V (.006% Rdg + 3 digits) 2-1000V (.005% Rdg + 3 digits)
6 mo., 23° ± 1°C	.2V (.01% Rdg + 5 digits) 2V (.008% Rdg + 4 digits) 20-1000V (.01% Rdg + 4 digits)
Temperature Coefficient After zero on .1V	(.0003% Rdg + 1 digit)/ C
Input Resistance	.2, 2, 20V ≥1,000 MΩ 100, 1000V 10 MΩ
Input Bias Current	<200 pA
Input Bias Current Temperature Coefficient	≤10 pA/°C
Normal Mode Rejection Filter Out Filter In	>40 dB @ 60 Hz, 23 dB @ 380 Hz >70 dB @ 60 Hz, 55 dB @ 380 Hz
Common Mode Rejection DC (500V max) AC (500 Vrms max)	>140 dB >120 dB
DC RATIO (DMM) Signal Input Range Ref. Input Range Signal/Reference Input Resistance Accuracy (Signal Range) After zero on .1V 24 hr., 23° ± 1°C	Same as DC volts 10, 100 volts Same as DC volts .2V (.012% Rdg $6\frac{RR^*}{RI}$ digits) 2-1000V (.01% Rdg $4\frac{RR^*}{RI}$ digits)

Table 1-2. Performance Characteristics (Continued)

PARAMETER	SPECIFICATION
6 mo., 23° ± 1°C	.2V (.02% Rdg + 10 $\frac{RR^*}{RI}$ digits) 2V (.016% Rdg + 8 $\frac{RR^*}{RI}$ digits) 20-1000 (.02% Rdg + 8 $\frac{RR^*}{RI}$ digits)
*Reference Range or 1 whichever is greater Reference Input	
Temperature Coefficient After zero on .1V	(.0006% Rdg + 2 digits)/°C
AC VOLTS (AVERAGE RESPONDENT) Ranges	2, 20, 200, 1000V RMS
Accuracy 6 mo., 23° ± 1°C for Inputs ≥ 500 Volts, add .1% of reading	30-50 Hz ±(.4% Rdg + 30 digits) 50-15 KHz ±(.1% Rdg + 20 digits)
Temperature Coefficient	(.005% Rdg + 2 digits)/°C
Input Impedance	1 MΩ in parallel with <200 pF
OHMS (2-WIRE) Ranges	.2, 2, 20, 200, 2000, 20,000 KΩ
Open Circuit Voltage	6V max
Accuracy After zero on .1V 24 hr., 23° ± 1°C 6 mo., 23° ± 1°C	 ±(.03% Rdg + 5 digits) ±(.03% Rdg + 6 digits)
Temperature Coefficient	.2 to 2000 KΩ ±(.01% Rdg + 2 digits)/°C 20,000 KΩ ±(.015% Rdg + 2 digits)/°C
Voltage Protection	260V RMS maximum input without damage
Short Circuit Current	<15 mA

Table 1-2. Performance Characteristics (Continued)

PARAMETER	SPECIFICATION
GPIB INTERFACE IEEE-488-1978: All ranges and functions programmable	Standard Interface Compatible Refer to Section 4 for GPIB Interface operation
GENERAL Read Rate	4 readings/sec
Power	100, 120, 220 or 240 V ±10% 25 watts, 45-450 Hz
Dimensions	3.5 in. x 14 in. x 16.75 in.
Operating Temperature Range	0° to 55°C
Storage Temperature Range	-40° to +70°C
Operating Humidity	<75% RH, 0° to 40°C <50% RH, 40° to 50°C
Maximum Voltage Input	All AC, all DC, all Ratio ranges; 1000 volts RMS max
Balance Time Filter In Filter Out	 Less than 4.5 sec Less than 2.5 sec

Table 1-3. Tools and Test Equipment

Function	Qty	Item	Minimum Use Specifications	Suggested Equipment
DC	(1)	Saturated Standard Cell Bank (6 cells)	1 ppm, certified	EPPLEY 106
	(2)	DC Voltages Sources	0.1 ppm resolution	FLUKE 332B
	(2)	Voltage Dividers, Adjustable	< 1 ppm linearity	FLUKE 720A
	(1)	Decade Resistance Box		ESI DB62
	(2)	Null Detector/μVoltmeters	1 μV sensitivity	FLUKE 845AR
AC	(1)	Thermal Transfer Standard	50 ppm	HOLT 6A, With corrections
	(1)	AC Voltage Source	1 ppm resolution	HP745A/746A
Ω	(8)	Resistance Standards	Known within:	
		100Ω	10 ppm	ESI SR1 with corrections
		1 KΩ	10 ppm	ESI SR1 with corrections
		10 KΩ	10 ppm	ESI SR1 with corrections
		100 KΩ	10 ppm	ESI SR1 with corrections
		1 MΩ	10 ppm	ESI SR1 with corrections
		10 MΩ	20 ppm	ESI SR1 with corrections
OTHER	(1)	Momentary Switch, SPST	–	–
	(2)	1.5 volt cells w/screwtype binding posts	–	–
	(1)	Insulated Adjustment tool	–	JFD5284
	(1)	100Ω, 10 Kilohm, 1 Megohm 1/4 Watt 5% Carbon Resistors	5%	–
	(1)	1 μFD non polar capacitor	–	–

Item	Minimum Use Specification	Calibration Equipment
1. DC Power Supply	Adjustable 0-20 VDC	–
2. Oscilloscope	25 MHz Bandwidth	TEK 454
3. DMM	0.1% DCV	Racal-Dana 6000

SECTION 2

INSTALLATION

2-1. PURPOSE. The Digital Multimeter Assembly 3102494 (DMM) is assembled at the factory and is a direct replacement for the CIMRON E9500-991B in the F-111 test stations.

2-2. UNPACKING AND INSPECTION. Prior to unpacking the instrument, examine the exterior of the shipping carton for any signs of damage (all irregularities should be noted on the shipping bill). Carefully remove the instrument from the carton's packaging and inspect the instrument for any signs of damage. Notify the carrier immediately if damage is apparent; bench test the unit if necessary.

2-3. RACK MOUNTING INSTALLATION. Remove all electrical power from the F-111 test station and tag circuit breakers and switches before removing the CIMRON Digital Multimeter and installing the 3102494 General Dynamics Electronics Division Digital Multimeter.

WARNING

Prior to installing the 3102494 General Dynamics Electronics Division Digital Multimeter all electrical power will be removed from the test station. External power disconnected switches will be locked out and "Danger-Do Not Energize - Men Working on Equipment" tag attached to prevent inadvertent energizing of the system.

To install the 3102494 Digital Multimeter proceed as follows:

a. Disconnect all external connector wiring from the CIMRON Digital Multimeter and tag the end connectors with the proper reference designator.

b. Remove the four front panel rack mounting screws of the CIMRON.

c. Remove the CIMRON chassis from the test station rack.

d. Remove slide rails from CIMRON chassis by removing three attaching screws on each slide rail, and install slide rails on 3102494 DMM chassis.

e. To install the 3102494 Digital Multimeter into the test station equipment rack, lift drawer (DMM assembly) into position in test station and engage the slides.

f. Connect ground strap from cabinet to left side of DMM drawer using ground strap bracket.

g. Install locking pin on rear of DMM cable control arm on station left rail assembly.

h. To install external connector wiring:

(1) Connect test station connector J3 to connector P3 located on the rear of the 3102494 Digital Multimeter.

(2) Connect test station connector J4 to connector P4 located on the rear of the 3102494 Digital Multimeter.

(3) Connect test station power connector J2 to connector P2 located on the rear of the 3102494 Digital Multimeter.

i. Push DMM drawer into the cabinet all the way, and install the four front panel rack mounting screws (removed from the front panel of the CIMRON in step b.) to retain the 3102494 Digital Multimeter in the test station.

2-4. ELECTRICAL POWER INSTALLATION. Electrical power is distributed from the F-111 test station through connector J2 on the digital multimeter to CB1 power ON-OFF switch. The CB1 power ON-OFF switch is located on the front panel of the digital multimeter and controls electrical input power to the digital multimeter interface and Racal-Dana DMM 5005-S-4622.

2-5. ELECTRICAL POWER ON. After familiarization with Section 4 Operation, apply electrical power to the Digital Multimeter Assembly as follows:

a. Apply power to the F-111 test station.

b. Position the DMM interface assembly CB1 power ON-OFF switch to ON (up) position (figure 4-3).

c. On the Racal-Dana DMM, depress the POWER switch (46) (figure 4-1).

2-6. PREPARATION FOR USE. Following Installation and Electrical Power-ON, exercise the F-111 test station Confidence test program. Successful completion of the Confidence test program will be followed by exercising the Maintenance program, when applicable.

SECTION 3

THEORY OF OPERATION

3-1. GENERAL. This section presents the circuit description for the Digital Multimeter Assembly 3102494 (DMM) as the signal propagates from the input terminals to the front panel display or the rear panel General Purpose Interface connector. The text will refer to simplified diagrams, schematics and other aids which may be required to enhance the general description.

The physical configuration drawing illustrated in figure 3-1 is an exploded chassis view which displays the DMM main sections comprising the main PCB. The numbers identified with each section are the discussion sequence followed in the text. A block diagram of the DMM is shown in figure 3-2.

3-2. POWER SUPPLIES. The DMM is designed to operate from a wide range of AC line voltages and frequencies with 120 VAC and 60 Hz considered standard. The transformer design includes a selectable multi-tapped primary winding to accommodate line voltages of 100, 120, 220, and 240 VAC ±10% from 47 through 440 Hz. A multi-tapped secondary with three separate windings develop the low voltage DC supplies required to power the DMM circuits.

The primary windings are wrapped with a shield, transformer terminal 6 and the shield is connected to the DMM chassis. The chassis is connected to power line ground through the power receptacle, J209. The analog windings have two additional shields for maximum isolation and common mode rejection. The guard shield, transformer terminal 18 extends through the analog section of the PCB with two aluminum shields guarding the analog circuits. The inner shield, transformer terminal 17, is connected to analog common.

From the three secondary windings, low voltage DC supplies are generated to power the main sections of the DMM. The voltage levels designators and grounds appearing on the power supply schematic 4310650 (Section 6) are used on all schematics; this is a sound troubleshooting aid.

3-3. SIGNAL CONDITIONING. The DMM is basically a DC voltmeter. Signal conditioning for functions other than DC volts is performed by the sections configured to convert AC volts or resistance values to a DC signal. The DCV scaling circuits and Isolator are utilized by ACV and ohms signal conditioning functions. The ACV and ohms signal conditioners are described in paragraphs 3-6 and 3-7. This group is assembled in Section 2, the Analog section of figure 3-1.

3-4. FUNCTION AND RANGE SWITCHING. The DMM's function and range are controlled by keyboard inputs, GPIB commands or Autorange. Upon receiving this signal, the microprocessor sends a new bit pattern to the function/range control shift registers in order to energize the proper relays and supply proper logic levels to other hardware.

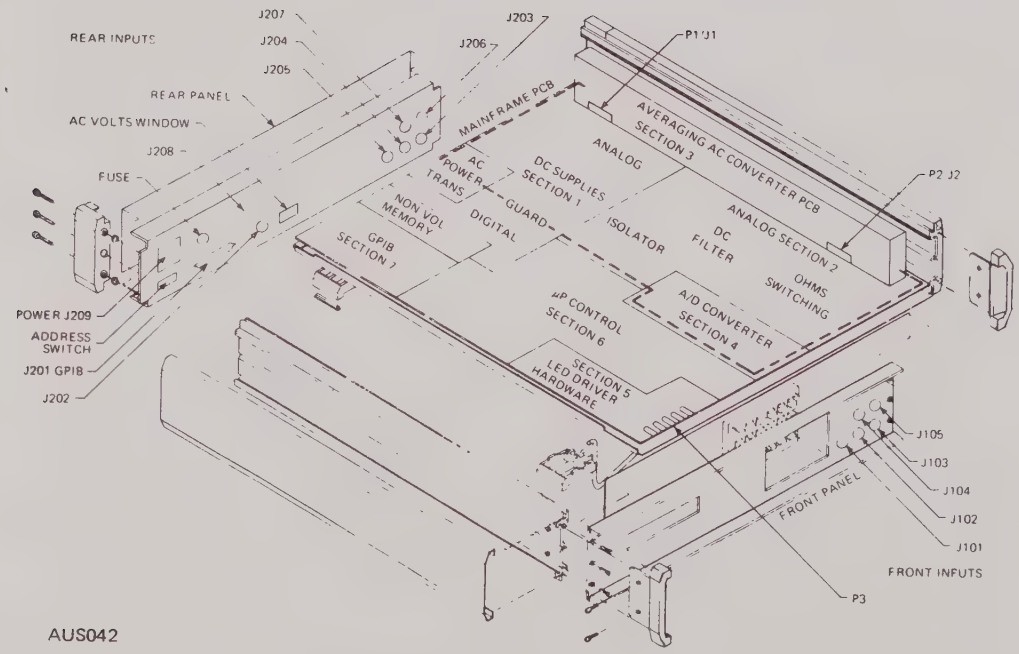

Figure 3-1. Model 5005 Physical Configuration

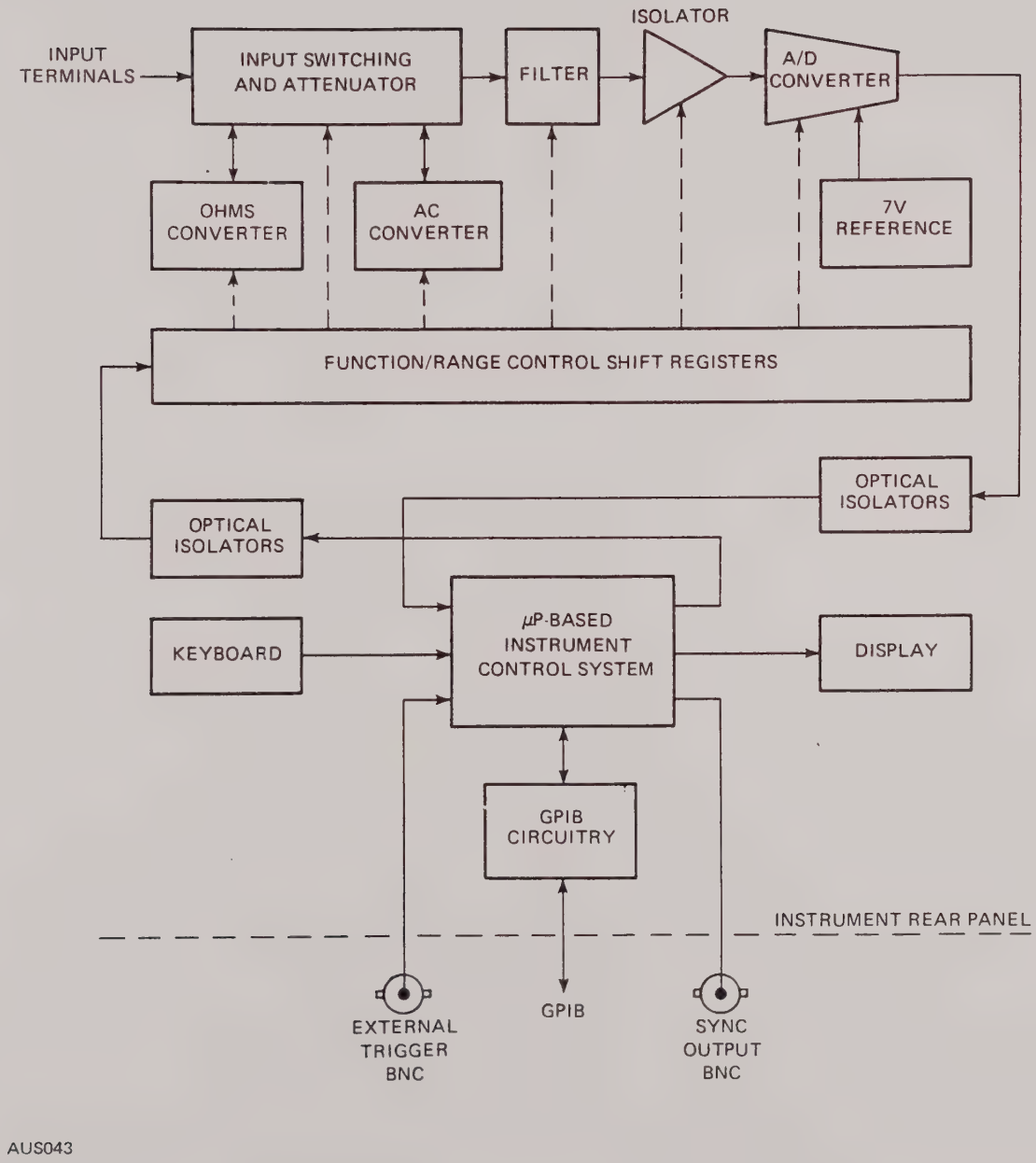

Figure 3-2. DMM Block Diagram

The active relays during the execution of the function logic are K1, K8, K11, and K12. The home state for K12 connects the DCV input from HI-LO input terminals directly to the attenuator. When the ACV function is enabled, K12 is energized, routing the input signal to the AC converter. In the ohms function, K1, K8, K12, and K11 are energized, switching in the ohms converter. The relay position for function and range modes are listed in tables 3-1 and 3-3, the shaded areas indicate the active relays.

3-5. DC VOLT FUNCTION. The DC volt mode performs three functions as the signal is conditioned for measurement: scaling the input signal to one volt full scale; filtering the signal to reduce unwanted noise; isolating the source from loading effects.

In the .1, 1, and 10 volt ranges, the measurand received from the HI-LO INPUT terminals, routed through the front-rear relay K13 is applied to the Isolator input. In the 100V and 1000V ranges, the attenuator is switched into the signal path when relay K9 is de-energized. This divides the voltage by 100, supplying the Isolator input with 20 volts maximum. The table 3-2 charts the voltage range, the scaling and the relay numbers which develop the resulting voltage. The DC over-voltage clamp consisting of a pair of zener diodes and regular diodes limits the isolator amplifier input voltage to ±24 volts maximum. The simplified diagram figure 3-3 illustrates the DC volts signal conditioner from the input terminal to the isolator output. The detailed schematic is in Section 6.

The Active Filter can be switched in or out of the circuit at the User's option. The filter configuration is a 3-pole active Bessel type formed by operational amplifier AR6 and capacitors C55, C45 and C58. The "FILTER" enables relay K10 through function and range logic, switching the 3-pole active filter into the circuit.

The Isolator amplifier configuration contains an input clamp, isolator amplifier, bootstrap amplifier, and a gain switching network controlled by the range and function logic. The various prescaled and processed input signals are applied to the isolator input. Input overloads are clamped at ±24 volts. The isolator is an operational amplifier consisting of AR9 and AR7 with a closed loop gain of 1, 10, or 0.1. The Isolator permits measurements from high impedance sources without introducing reading errors. The isolator accepts either positive or negative voltages at its input up to ±20 volt maximum, and provides outputs up to ±2 VDC maximum, controlled by the range logic. The isolator gain switching is effected by Q15, Q16 and Q17 which when enabled, switch different value resistors across the isolator feedback network. The chart in figure 3-4 illustrates Isolator gain switching. The bootstrap amplifier AR8 senses the isolator feedback voltage and supplies the +BSV (bootstrap voltage), -BSV, the input and bias current network. The purpose of the bootstrap amplifier is to provide the isolator amplifier with supply voltages which are centered around the input signal to the amplifier, varying approximately 6 volts higher than the isolator input (+BSV) and approximately 6 volts lower (-BSV).

3-6. OHMS FUNCTION. In the Ohms function, the ohms converter generates a fixed and stable current for each range selected. The current is fed through the resistance to be measured, with the voltage drop across the resistor proportional to the resistance. This voltage is read by the DMM and displayed as kilohms on the display. The current supplied provides a full-scale DMM reading when the unknown resistance is equal to the range selected. For example, the measuring of 10 kilohms on the 10 range produces a DMM readout of 10.0000.

Table 3-1. Function Relay Chart

FUNCTION	K1	K8	K11	K12
DC				
AC				
OHMS				

ENERGIZED

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Table 3-2. Isolator Range Chart

RANGE	K9 ÷ 100	Q16 X1	Q15 X10	Q17 ÷ 10
.1V				
1V				
10V				
100V				
1000V				

RELAY ENERGIZED OR FET SWITCH ON.

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Table 3-3. Range Relay Chart

FUNCTION	RANGE	K2	K3	K4	K5	K6	K7	K9
DC	.1V							
	1V							
	10V							
	100V							
	1KV							
AC	1V							
	10V							
	100V							
	1KV							
OHMS	.1KΩ							
	1KΩ							
	10KΩ							
	100KΩ							
	1000KΩ							
	10,000KΩ							

ENERGIZED

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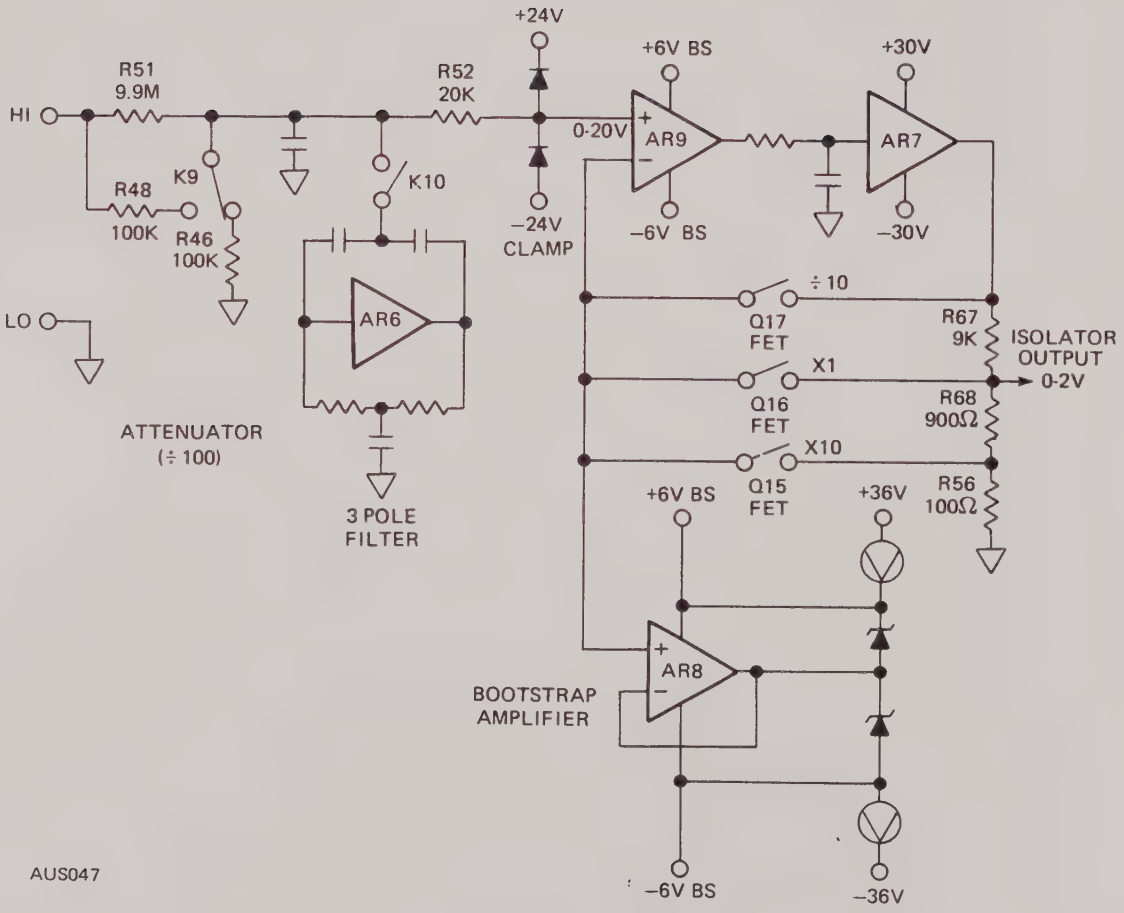

Figure 3-3. DC Volts Signal Conditioner

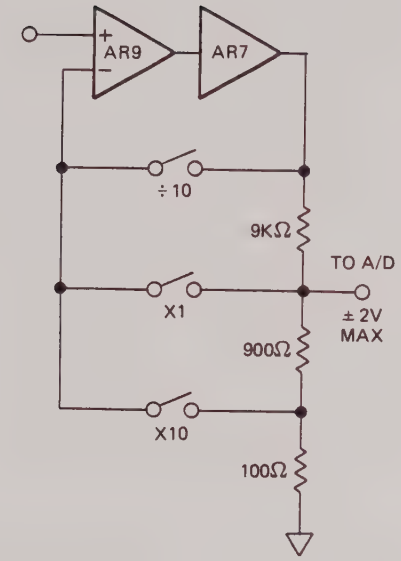

Figure 3-4. Isolator Gain Switching

Table 3-4. Ohms Range, Relay and I Source

RANGE	K2	K3	K4	K5	K6	K7	CURRENT SOURCE
.1K					■	■	10ma
1K					■		1ma
10K	■		■				1ma ÷10
100K		■	■				1ma ÷100
1000K			■				1ma ÷1000
10000K				■			1ma ÷10000

■ ENERGIZED

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The Ohms Converter utilizes an accurate reference voltage generator to generate a reference current source through the resistor divider and current switching network, refer to figure 3-5. An open input-clamp is also part of the ohms converter circuit. The ohms voltage reference is a precision temperature-stabilized zener, LM3999, with a 5 ppm/°C temperature coefficient. It includes internal circuitry that reduces the zener's dynamic impedance to 0.5 ohms. This feature permits the zener to operate from 0.5 mA to 10 mA with no change in voltage. The 7 volt reference is buffered by the ohms current source generator op-amp AR1. The current through darlington transistor pair Q7 and Q8 is determined by R31 and R35. This network supplies 1 mA or 10 mA to the resistor-divider network. Relay K7 switches R35 in parallel with R31 to generate the 10 mA current source. The ohms ranges, current sources, and the range-logic controlled relays are shown in table 3-4. The open-input clamp protects the user's external input from voltage increases when the ohms terminals are not provided with a resistive load, or during range overload. The input open circuit voltage is clamped at -6 volts maximum by Q3, Q5, and transistor array U3. U3 clamps the base of Q7 to -30 volts thereby turning off the current source through Q8 during overload.

The Ohms Measurement System presented in the simplified drawing figure 3-6, sources a known current through the unknown resistor and reads the voltage drop across the resistor which is transposed to ohms on the display. The circuit contains an input clamp Q4 and Q2 limiting the drive to the differential amplifier Q1, a matched pair of FETs with very high input impedance and low bias current. The ohms amplifier output is routed to the Isolator (+2 volts maximum). The amplifier output is protected from over voltage inputs when the ohms function is accidentally used for voltage readings by clamp CR1, Q6 and VR4 which clamps at +3 volts and -0.6 volt. CR2, Q8, and VR3 protect the current source from voltages applied at the input terminals.

3-7. AVERAGING AC CONVERTER. The AC Converter is assembled on a separate printed circuit board and occupies connectors J1 and J2 on the circuit board at Section 3 of figure 3-1. The converters accept AC inputs on the 1, 10, 100, and 1000 volt ranges, then scale and rectify these signals to produce a DC level representative of the input. With AC function selected, the AC input signal is routed from the input terminal to pin 2 of J1 (the remaining five pins of J1 are used as a shield); the resultant DC output from pin 2 of J2 (-1 volt for a full-scale input) is routed to the isolator.

The averaging converter shown simplified in figure 3-7, consists of an active rectifier/range circuit, a filter, and an output amplifier. The active rectifier is an operational amplifier with two polarity sensitive feedback paths; the feedback path consisting of CR3 and R29 conducts current when the output of the amplifier is positive and the CR4, R28 path conducts when the amplifier is negative. The two currents are recombined across resistor R30, and the resulting AC signal is fed through the range feedback network to the input summing node of the operational amplifier. Two half-wave signals of opposite polarities are developed across resistors R28 and R29 for each full-wave input. These signals are filtered and amplified as a DC level by the differential output amplifier. Feedback on the 1 volt range is through a permanently connected feedback path; the 10, 100, and 1000 volt ranges have relay selected feedback paths that parallel the 1 volt network, through K1, K2, and K3.

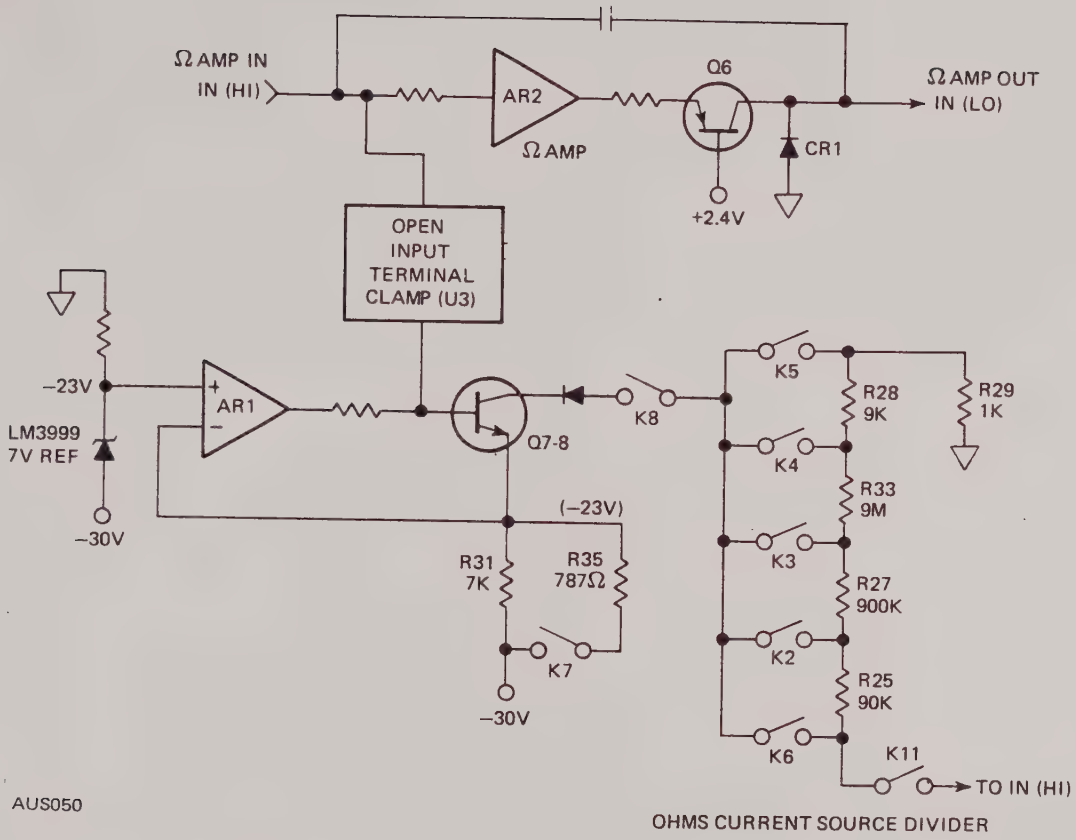

Figure 3-5. Simplified Ohms Converter

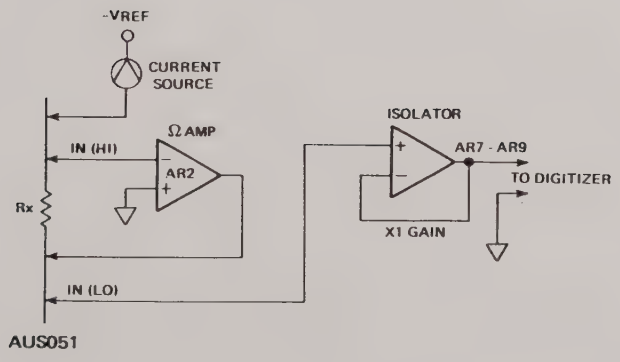

Figure 3-6. Ohms Measurement System

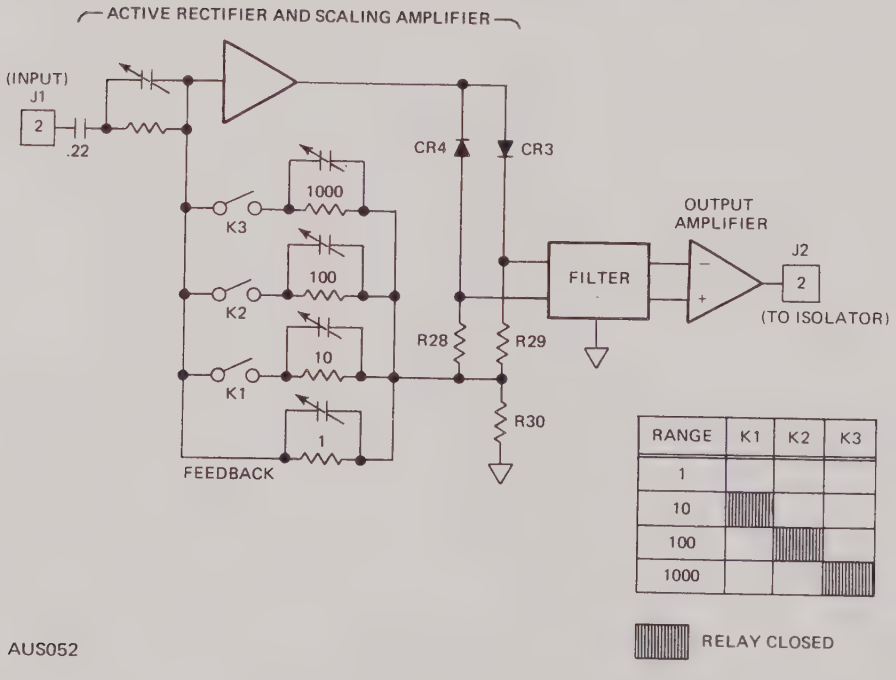

Figure 3-7. Averaging AC Converter

3-8. QUANTIZED FEEDBACK A/D CONVERTER SYSTEM.

3-9. General. The Quantized Feedback analog-to-digital converter performs the measure and count functions simultaneously in a fixed time interval, converting the analog input as applied. The Quantized Feedback (QF) measurement period is compared to Dual-Slope in figure 3-8. The control logic counts the up-down (U/D) control pulses, and the digital processor prepares the data in 4 bit BCD format, one digit at a time. The QF design inherently develops auto-zero and auto-polarity features.

The A/D assembly consists of the Digital control and counter LSI chip U10, and QF analog converter chip U11, with the support components: measure/zero (M/Z) switch U26, input buffer amplifier AR5, voltage reference VR1, output opto-isolator drivers U17 and U9, and auto-zero buffer circuit Q9 and AR3. This assembly occupies section 4 on the PCB, refer to figure 3-1.

3-10. Digitizer Control Processor and Counter. The Digitizer Control chip U10 has an internal timebase generator which allows the converter output to be synchronized with the DMM microprocessor control. This feature allows front panel control by the operator. The A/D converter control logic signals shown in figure 3-9 are designated as follows:

a. Output from U11

COMP: Comparator's digital output comparing the input voltage and the reference voltage.

b. Outputs from U10

(1) M/Z: Enables and clocks the measure interval and the auto-zero interval.

(2) U/D: Up-down counter control clocks the analog switch's high and low periods during the measure and auto-zero intervals.

c. Inputs to U10

(1) DIGIT MODE: Select the DMM 5-1/2 or 4-1/2 digit operating mode.

(2) START TRIGGER: Allows the microprocessor to trigger the A/D to take a single reading or a series of readings.

3-11. Quantized-Feedback Basics. The converter's simultaneous measure and count principle utilizes three voltages summed at the integrator input node 9. Refer to simplified A/D converter diagram figure 3-10, this illustrates the designators and pin numbers associated with the components depicted on the detail schematic, 431650-5 (Section 6).

The three voltages, scaled by resistors R22, R20, and R9 are:

a. The analog voltage 'Vin', which varies from 0 to ±2 volts full scale.

b. The reference voltage 'Ref'. The U/D duty cycle applies '0' volts or 7 volts from the 7 volt reference.

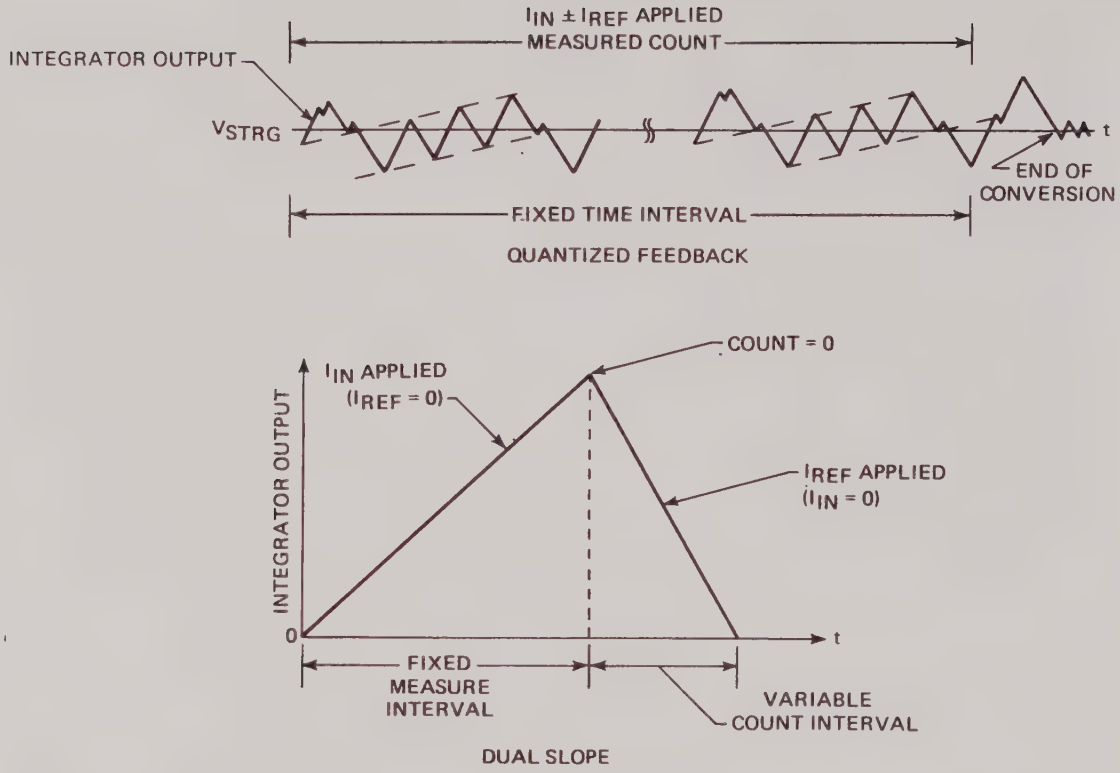

Figure 3-8. Measurement Period Comparison - Quantized Feedback Versus Dual Slope

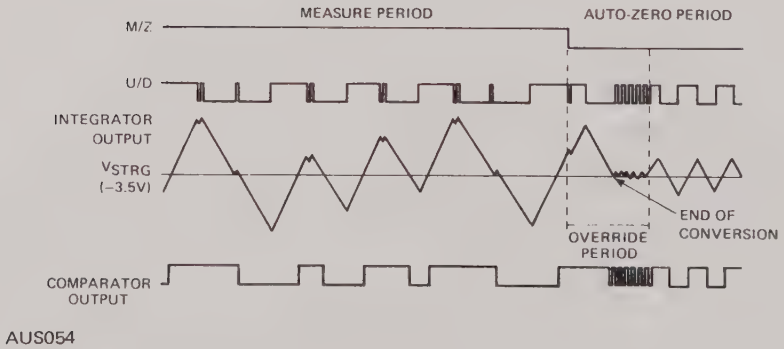

Figure 3-9. Typical A/D Converter Waveforms

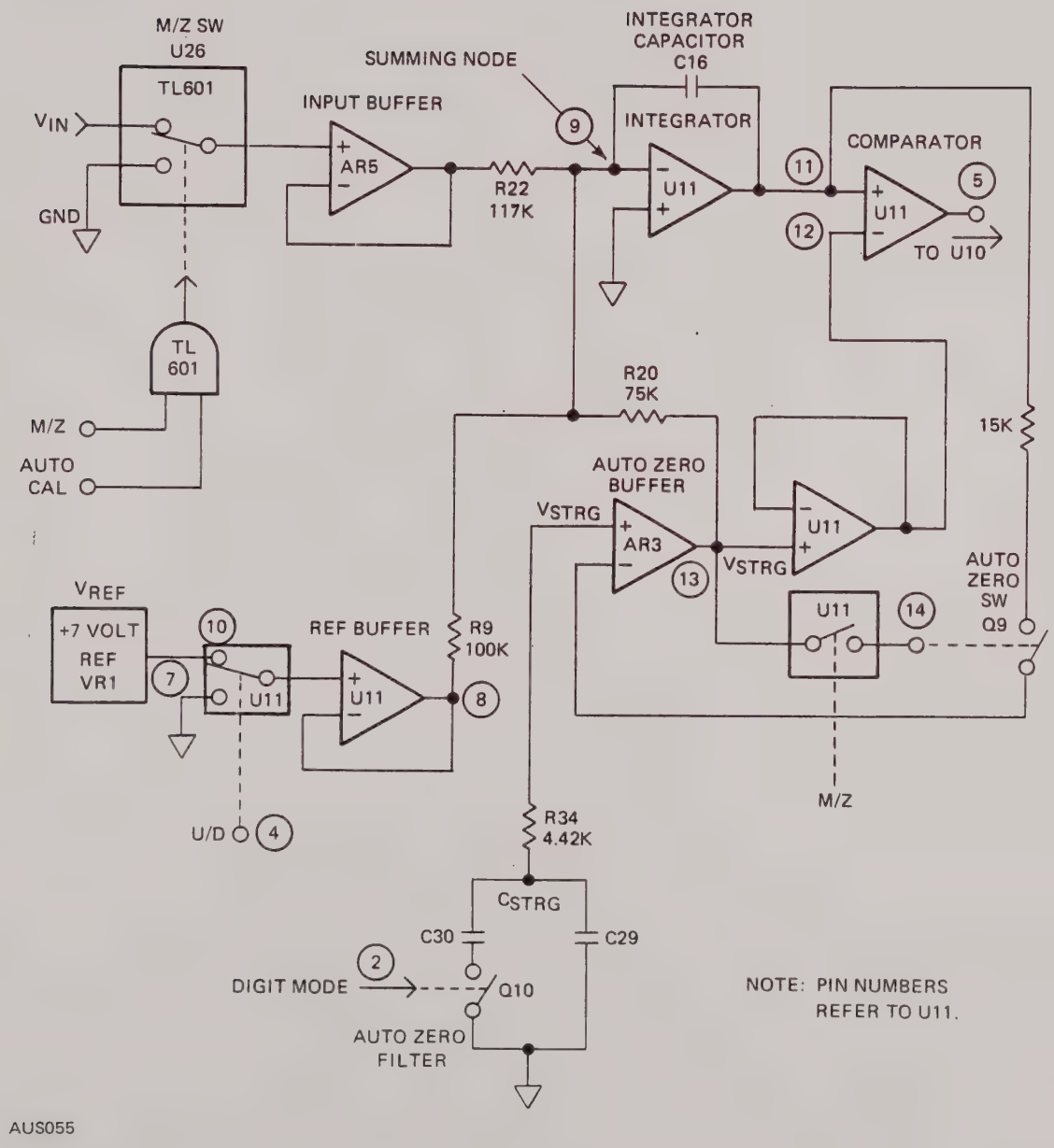

Figure 3-10. Simplified A/D Converter Diagram

c. The storage voltage 'Vstrg'; voltage developed across AZ capacitor 'Cstrg', the -3.5V average integrator output during auto-zero.

The working relations for the three voltages are examined with the descriptions of the auto-zero interval and the measure interval.

Timing: A time base generator divides the 2-phase clock into sampling periods of 614,400 of which 409,600 pulses are the measure interval and 204,800 pulses are the auto-zero interval. The up-down (U/D) counter, and the AZ interval averages zero, with 80 counts down and 80 counts up. The Measure Zero interval sample waveforms are reproduced in figure 3-9. During the measure interval, the U/D counter nets 140 counts. When the comparator output is high compared to Vstrg, U/D counts up 10 and down 150, when low, the U/D counts up 150 and down 10 during the 160 clock cycle period.

3-12. Auto-Zero Routine. The M/Z logic grounds M/Z switch U26, and inhibits the input analog signal Vin. The Input Buffer AR5, with zero input contributes only offset voltage to the summing node (pin 9 on U11) through R22. The U/D buffer is toggled by the control logic between the voltage reference, U11 pin 10 and ground. This results in a reference current flow to the summing node half of the time. The AZ capacitor Cstrg, C29 and C30, assume Vstrg voltage that is equal to the average of the integrator output (-3.5V). The AZ buffer AR3 supplies a current to the summing node equal to the voltage Vstrg divided by R20 (75K).

The system will reach a balance when the sum of DC currents into the summing node equals zero. Capacitor Cstrg "stores" Vstrg voltage when the AZ switch opens at the end of the auto-zero interval. The digital BCD counters are disabled during the AZ interval, but are reset to zero by the last clock pulse from the AZ interval.

3-13. Measurement Interval. During the measurement interval the U/D level starts low and the U/D controlled reference buffer is switched to Vref. In this state, positive voltage sums at the integrator capacitor C16. A high level toggles the U/D buffer to ground, and in this state, negative voltage sums at C16. In one cycle, charge is either added to or subtracted from the integrator capacitor. The BCD counter is decremented (-140 counts) for each addition and increment (+140 counts) for each subtraction of quantized charge.

The measurement interval logic also switches the M/Z switch U26, enabling input buffer AR5 which accepts the isolator output signal of 2 volts, maximum. The input buffer routes the analog voltage to the integrator causing the integrator output to vary from Vstrg; stored during the last AZ interval. The control logic attempts to keep the integrator near Vstrg by adding or subtracting quantized charge to the integrator capacitor C16. The net amount of reference charge required to balance the input voltage charge at the input of the integrator is totaled by the BCD counter in U10. The BCD count at the end of conversion equals the number of charge parcels necessary to cancel the input voltage and the resulting digital count is proportional to the analog voltage.

Integrator Input Terms	$\frac{Vin}{(+2V)}$	+	$\frac{Vstg}{(-3.5V)}$	+	$\frac{Vref}{0V}$	=	Digital Converter Output
	(-2V)	+	(-3.5V)	+	7V	=	Digital Converted Output

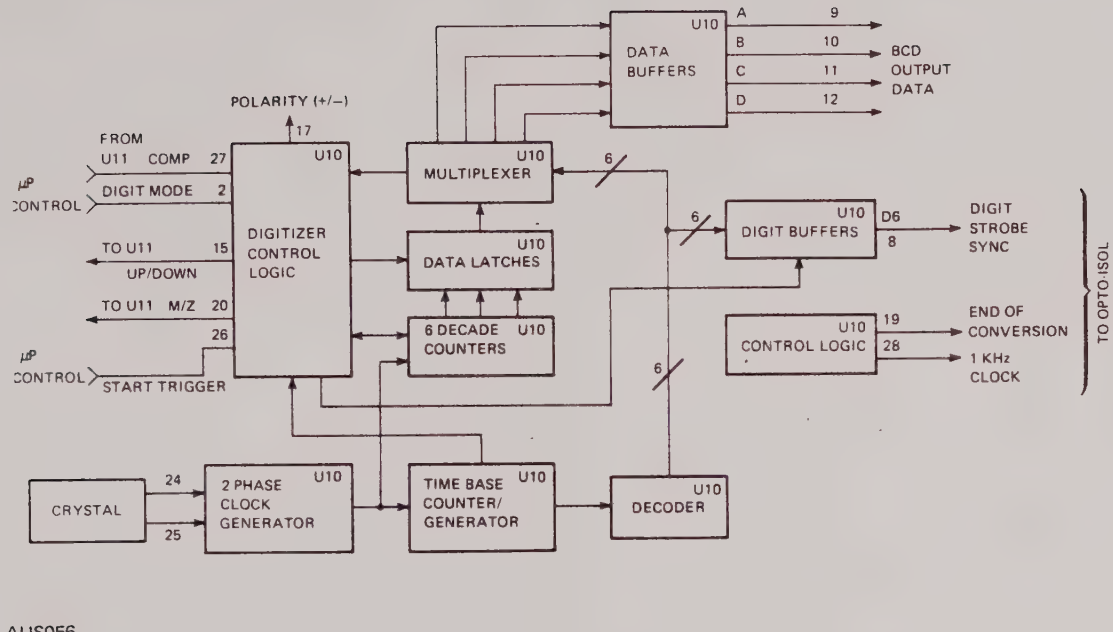

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Figure 3-11. A/D Digitizer Control and Counter

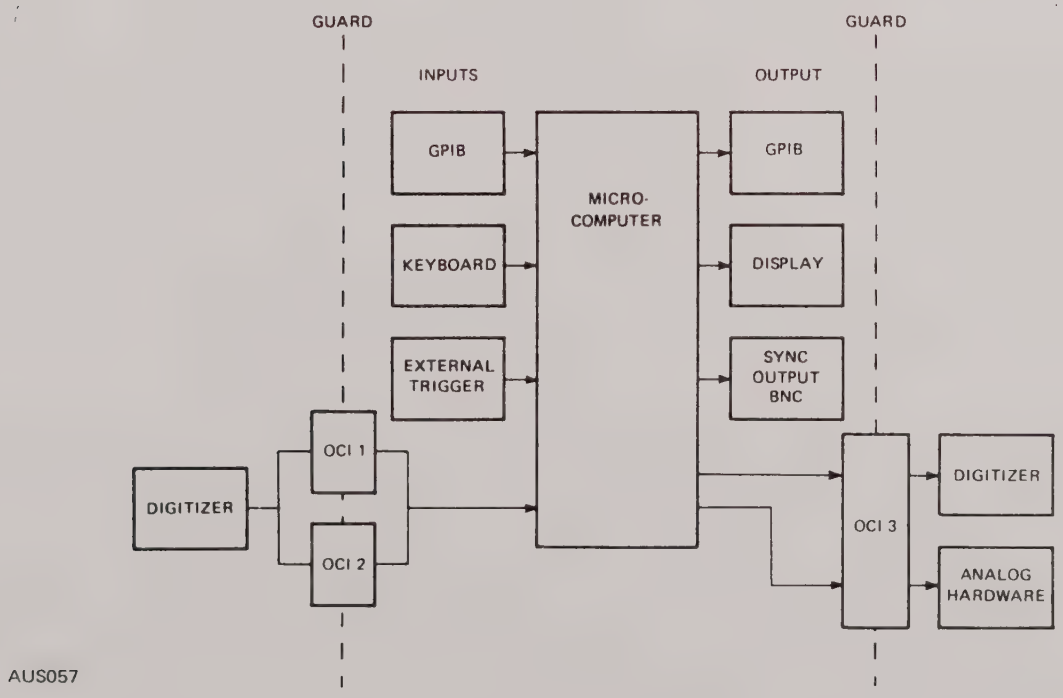

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Figure 3-12. Main Inputs to and Outputs from the Model 5005 Microcomputer

3-14. Digitizer Control and Counter Output. The 4 bit BCD data stored in the data latches are multiplexed and routed through the opto-isolator drivers U9 and U17, and presented one digit at a time to the microprocessor control section of the DMM.

The other A/D output control signals are:

a. END OF CONVERSION: Advised microprocessor that A/D conversion is completed and that a reading is ready.

b. 1 KHz: Synchronizes data transfer between A/D and microprocessor.

c. DIGIT STROBE SYNC: Advises microprocessor when the first BCD digit is being transmitted.

d. POLARITY: Polarity information passed onto the microprocessor (+ or - input).

3-15. DIGITAL THEORY OF OPERATION.

3-16. Digital Hardware Description. The Model 5005 digital control centers around U35, a 6802 microprocessor which executes the program contained in ROMs, reads data from various locations throughout the DMM and stores data to RAM and to various hardware locations throughout the DMM. The microprocessor executes the ROM program based on these data, performs calculations, and makes decisions to control all the functions described in Section 4.

The hardware locations contributing data to the microprocessor are the Digitizer (via opto-couplers OCI1 and OCI2), the keyboard on the front panel, and through the GPIA (U44) which passes commands from the 488 bus to the microprocessor.

In turn, the microprocessor outputs processed data to the GPIA and LED display. The microprocessor also sends control information to the Digitizer and the analog hardware via opto-isolator OCI3. Figure 3-12 graphically presents the hardware network controlled by the microprocessor. The schematic drawing 431650-7 listed in Section six presents the coded designators that input and output to/from the microprocessor through the opto-couplers.

3-17. The Microprocessor Section. The microprocessor section (MPU) located in section 6 on the motherboard consists of the microprocessor U35, with program memory ICs U27, U28, U29, U30 and U31, address decoders U14 and U15, interrupt control hardware U2, U6 and U20, and non-volatile memory system U43, U42, VR12. BT1, and Q21. The complete schematic drawing 431650-6 is given in Section 6.

When power is first applied to the microprocessor, the R76-C75 time constant on the microprocessor's RESET input (U35-40) holds the microprocessor in reset long enough for the power supplies and clock to stabilize, then reset goes high (HI) enabling the start-up routine.

The DMM system clock is generated by the microprocessor combining internal components with external components connected to pin U35-38 and U35-39 comprising of a 3.579 MHz crystal Y1 and C73-C76 components. The microprocessor divides this frequency by 4 then outputs at pins U35-37 as 'E' the system clock of 895 KHz (rounded) for all microprocessor bus components.

3-18. Program Memory. The entire program memory for the microprocessor resides in ROMs U27 through U30. ICs U27, U29, U28, and U30 are connected so that all can hold a 2K x 8 model 2716 EPROM or U29 and U30 can be omitted and U27 and U28 can each contain a 4K x 8 ROM. The microprocessor directs other hardware locations dedicated to specific memory assignments as the Non-Volatile-Memory; GPIA and Digitizer.

3-19. Address Decoding. The ICs U14 and U15 comprise the address decoding hardware used by the microprocessor. The inputs to the address decoders are various address lines from the microprocessor as well as other control lines. Each decoder has 8 normally high outputs, AY0 to AY7 and BY0 to BY7, which are used as 'Chip selects' for various hardware throughout the DMM. When the microprocessor places an address on its address bus, U14 and/or U15 decode this address and supply the required chip select to the selected component which is being addressed by the microprocessor.

The outputs of U14 are not gated internally with the clock, therefore the negative pulse widths may vary from 900 to 1200 ns. The outputs from U15 are internally gated with the system clock E, therefore the outputs are practically a consistent pulse of 516 ns.

3-20. Non-Volatile Memory. The DMM uses a non-volatile memory (NVM) to store calibration (CAL) constants for later recall. The constants are stored during laboratory calibration and are recalled from the NVM whenever the DMM Function or Range is modified. The NVM is comprised of U43, a CMOS RAM, and Quad Nand gate U42 along with a 3 volt lithium battery BT1, a sharp knee zener VR12, a constant current regulator Q21 and steering diodes CR19 and CR21.

During normal DMM power-on operation, the NVM circuit receives 9 volts unregulated from the digital power supply. The current from the unregulated supply is regulated by Q21, a FET connected as a constant current source. This constant current (normally 7-13 mA) forward biases diode CR17 and causes VR12 to zener at approximately 5.3 volts. The voltage across VR12 reverse biases CR21 to prevent battery charging, and also supplies a regulated voltage to U42 and U43.

During the AC power-off periods, battery BT1 causes CR21 to forward bias so that approximately 2.5 volts is available to power U42 and RAM U43. This same voltage reverse-biases CR17 which prohibits battery flow into the power supply. When in this mode, approximately 2.5V is across VR12, the sharp zener. Because of its sharp knee feature, VR12 draws insignificant current, approximately 5 microamps at room temperature.

A hardware Write-Protect circuit prevents accidental modification of the contents of RAM U43 during normal operation, power up or down cycles and power brown-outs. This circuit is comprised of W/R control gate U42, a 10K pull-up resistor R79 and CAL-switch S1 which is located behind the front panel; refer to figure 4-1, (8). When the switch is open, pin 14 on RAM U43 constantly remains HI, which prevents any RAM "write" operation so that its contents cannot be modified. When the CAL switch is depressed, the microprocessor can drive the WRITE pin on the RAM LO, enabling the U43 memory modification.

3-21. Interrupt Control Hardware. The interrupt signals to the microprocessor are processed by the interrupt control hardware consisting of dual Flip-Flop U2, two NAND gates in U6, and 1/6th of inverter U7.

The interrupts from the Digitizer and GPIA are NANDED by U6-4, 5, 6, and inverted by U7-3, 4, to appear on the interrupt request (IRQ) pin of the microprocessor U35-4. This ANDing either from the Digitizer via the lower half of U2 or an interrupt from the GPIA via pin U6-5 will cause an interrupt to be gated to the microprocessor.

External Triggers from the rear panel BNC connector J202, drive pin U6-2 LO then are inverted by U6 causing a positive edge at pin U2-3. This trigger clocks a LO at pin U2-5 which will cause a non-maskable interrupt (NMI) to occur at the microprocessor pin U35-6. This NMI will cause the microprocessor to cease its present software calculations and act upon the external trigger. The number of triggers arriving at the microprocessor determine whether the microprocessor will re-enable the external trigger or not. Enabling the external trigger occurs by the microprocessor pulling pin U2-4 LO momentarily. If this is done, that portion of U2 will be set so that a second external trigger can be received by the hardware. If this is not done by the microprocessor as would be the case when many external triggers are received rapidly, then pin U2-5 will remain in a LO state until the microprocessor decides to pull pin U2-4 momentarily LO to set that half of U2.

The Analog Interrupts which originate from the analog side of the DMM are used to clock the lower half of U2. These evenly timed interrupts occur every 6 ms (every 7.2 ms in 50 Hz DMM) and clock the lower half of U2 at pin 11. This causes pin U2-9 to go LO, which causes the microprocessor's IRQ input to go LO. When the microprocessor responds to this interrupt, it reads the output of U20, a hex three-state buffer. Since pin U2-9 is connected to pin U20-10, the microprocessor can determine if the IRQ originated from U2 by examining the D7 output (pin 9) from U20. If U2-9 is found to be low, the microprocessor applies a negative pulse to pin U2-10, which removes the IRQ.

The interrupts which occur approximately every 6 ms as a result of the clock on pin U2-11 are used by the microprocessor to sequence the scanning of the keyboard and to check whether certain front panel LEDs need up-dating. If problems are observed in any of these areas, then a correct clock into pin U2-11 should be verified.

3-22. The Hardware Control Codes. The hardware which brings information from the analog section of the DMM to the digital section is presented in schematic drawing 431650-7 (Section 6).

The eight signals entering from the left edge of schematic 431650-7 are brought in from the analog section of DMM through the opto-isolator couplers OCI-1 and OCI-2 to the digital three-state hex buffer U16. Four of these are multiplexed (MUX) BCD data lines A, B, C, D lines. Via these lines, 6 digit MUX BCD data is brought across guard through the opto-isolators. The other four lines are single lines designated as follows:

a. POLARITY: This line indicates the polarity of the most recently completed reading.

b. 1 KHz: This line supplies a 1 KHz frequency (0.833 KHz in 50 Hz DMM). The high-low transactions of the 1 KHz waveform are monitored by the microprocessor to determine when a new BCD digit is being MUX across guard on the A, B, C, D lines.

c. DIGIT STROBE SYNC D6: This line is used to generate real-time interrupts to the microprocessor which was described previously and to help MUX the sign (polarity) bit into the microprocessor.

d. EOC: (END OF CONVERSION) This line changes state when a new reading has been completed. After crossing guard the EOC line is buffered by TTL Schmitt inverter (sections of U7) and is used to clock the input of the dual F/F at pin U8-11. When the F/F is clocked, the output pin U8-9 goes HI. This high output is read by the microprocessor and indicates to the microprocessor that a new reading is ready. The buffered output of the opto-isolator also goes, via U7 and U6 TTL buffer, to the display board and is used to drive the "sample" LED. Refer to figure 4-1 for the sample LED location.

When operating on 5-1/2 digit mode, the microprocessor spends considerable time waiting for a new reading to become available for process and display. It determines when a new reading is available by reading pin U8-9 via U13, the keyboard three-state hex buffer. When the microprocessor reads U13-3 HI, it then knows that a new reading is available and it begins to read the six digits which are constantly MUX across guard through opto coupler OCI-2. The microprocessor reads the MUX BCD pulses and other control lines through U16 a three-state hex buffer.

A typical set of waveforms are presented in figure 3-13 as they would appear to the microprocessor while reading the MUX BCD data from the analog section, crossing guard, to the input of U16. The microprocessor uses the positive edge of the 1 KHz signal to indicate when it should read the next nibble of BCD data from U16 inputs. The microprocessor uses the DIGIT STROBE SYNC D6 signal to indicate when the most significant digit is MUX across guard.

The LO DIGIT STROBE SYNC D6 signal also causes that the "sign" bit to be substituted in place of the D bit at U16's input. This switching of the sign bit in place of the D bit is done via the wired OR connection between the open collector outputs of OCI2 pin 10 and OCI1 pin 15.

3-23. Analog Control Registers. The analog hardware is housed in section 2 on the motherboard. The principal schematic 431650-4 (Section 6) presents a relay operation chart and circuit details.

The analog control system is comprised of a 4 bit latch U32, two shift registers U33 and U34, two relay drivers U18 and U19, relays K1 through K13, schmitt trigger U25 and isolator gain switch U36, as shown in figure 3-14.

The microprocessor program controls the digitizer, function, and range relays through 3 registers, 2 of which U34 and U33 are located on the analog side of guard, with the third U32, located on the digital side of guard.

U32 is a 4 bit latch which is loaded from the microprocessor's data and address bus. The output from U32 is used to load registers U34 and U33 as well as trigger the digitizer shown on schematic 431642-5.

3-24. U34/U33 Register Load. The DMM's function, range and/or integrate time can be modified as a result of keyboard inputs, GPIB commands, or AUTO range. When this occurs, a new relay drive bit pattern is determined by the

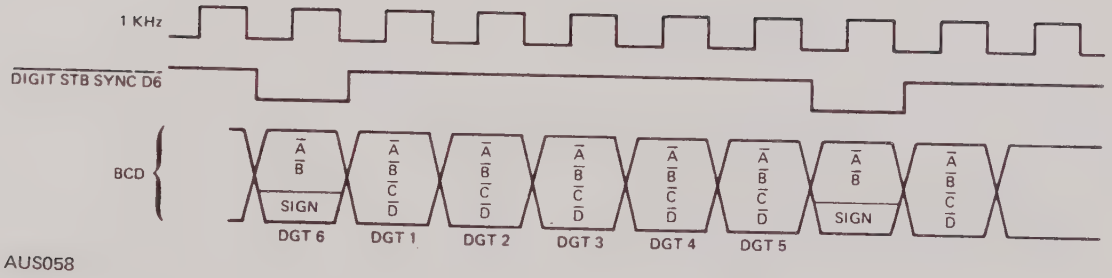

Figure 3-13. Typical Waveforms from Across Guard as Seen by Microprocessor Via Inputs on U16

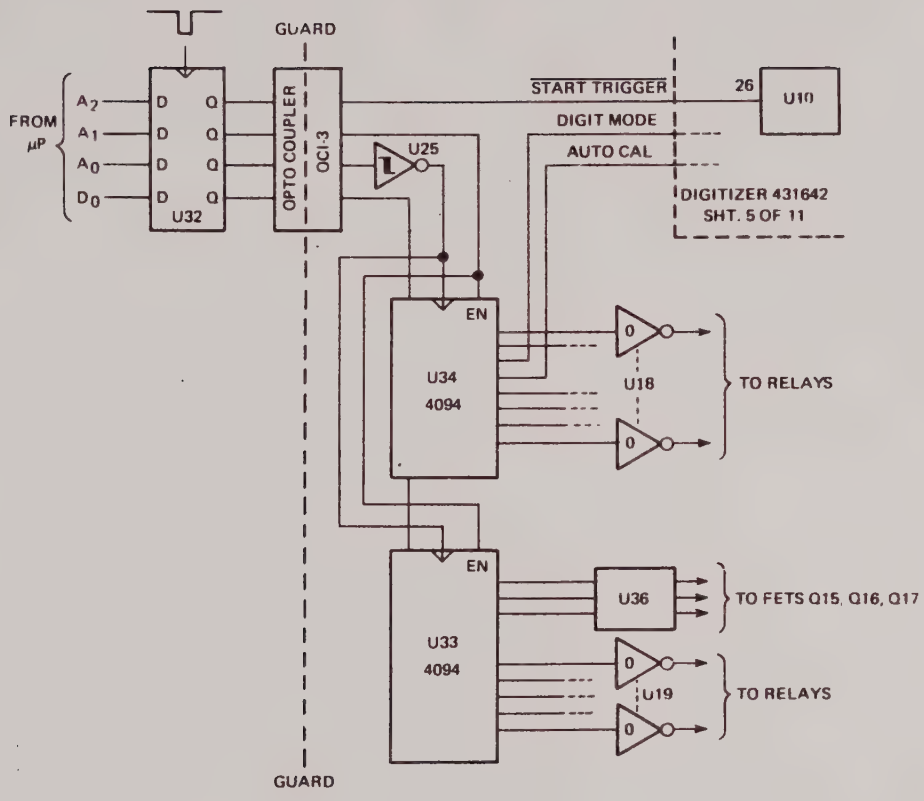

Figure 3-14. Analog Control Registers

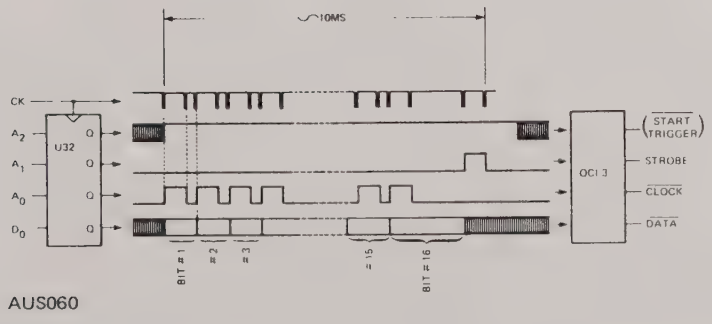

Figure 3-15. Register Load Simplified Timing Diagram

microprocessor. This pattern is then shifted across guard one bit at a time. The timing of the drive bit pattern is shown in figure 3-15, the Register Load Timing diagram.

The first bit of this pattern, with other control signals is latched into U32 from the microprocessor's data bus and address bus. After propagating through the relatively slow opto coupler OCI-3, the data bit appears at the 'D' input of U34, with a LO signal at U34's clock input. The microprocessor then stores the first bit to U32 along with other control signals that after progating through the opto coupler, the first data bit remains at U34's 'D' input with a "HI" signal at U34's clock input, which causes the first data bit to be shifted into U34. This sequence is repeated until all 16 bits have been shifted into U34 and U33, which requires about 10 milliseconds.

After shifting all 16 bits into U34 and U33 the microprocessor then strobes the shifted bits into the output registers of U34 and U33. To do this the microprocessor stores a control bit pattern to U32 which propagates through OCI-3 and places a high level on U34-1 and U33-1. About 0.3 ms later, the microprocessor removes this signal.

The output bits from U34 and U33 then energize relays via the open collector drivers U18 and U19, control Isolator gain via U36, or control the digitizer.

3-25. Digitizer Triggering. When the microprocessor requires a reading, it loads U32 with address line A2 LO. This then appears at U32's output, propagates across guard, and places a low level on pin 26 of U10 (digitizer drawing 431642-5, Section 6) to cause a read cycle.

When in the hold mode and at other times, the microprocessor waits for verification of a digitizer trigger by watching for a LO on pin 10 of U13, the keyboard buffer on drawing 431650-10, Section 6.

When operating in the "track" mode (internal trigger), the microprocessor leaves a LO on U10 pin 26 almost all the time in order to cause continuous triggers.

3-26. Keyboard Theory of Operation. The DMM's keyboard is located on the display PCB. The associated ICs are located on the motherboard and referred to as section 6 on the sectional chassis layout. Details are given on schematic drawings 431650-10 and 431651-1, Section 6.

The keyboard circuitry consists of MB-U5, an open-collector inverter used to buffer the microprocessor's address lines which drive the N, M, L, H, K, and J columns of the keyboard. The keyboard buffer U13 is a three-state buffer connected so that the microprocessor can read the signal from the keyboard rows T, R, U, and S. The pull-up resistor network Z2 pins 3 through 6 ensures that the microprocessor will read a HI from U13 if its inputs become open, a condition that exists when no key is pressed. The chip select for U13 is DSPE, which is the same chip select for U12. This chip select originates from the NAND gate output U6-8. See the DISPLAY test paragraph for further explanation.

The OPERATION is described as follows. When the microprocessor must determine if any key is pressed, it reads from U13 while address lines A0-A5 are high. The ones on A0-A5 lines propagate through U5 and appear as zeros on N, M, L, H, and J columns of the keyboard as shown in figure 3-16. When a key is pressed, the

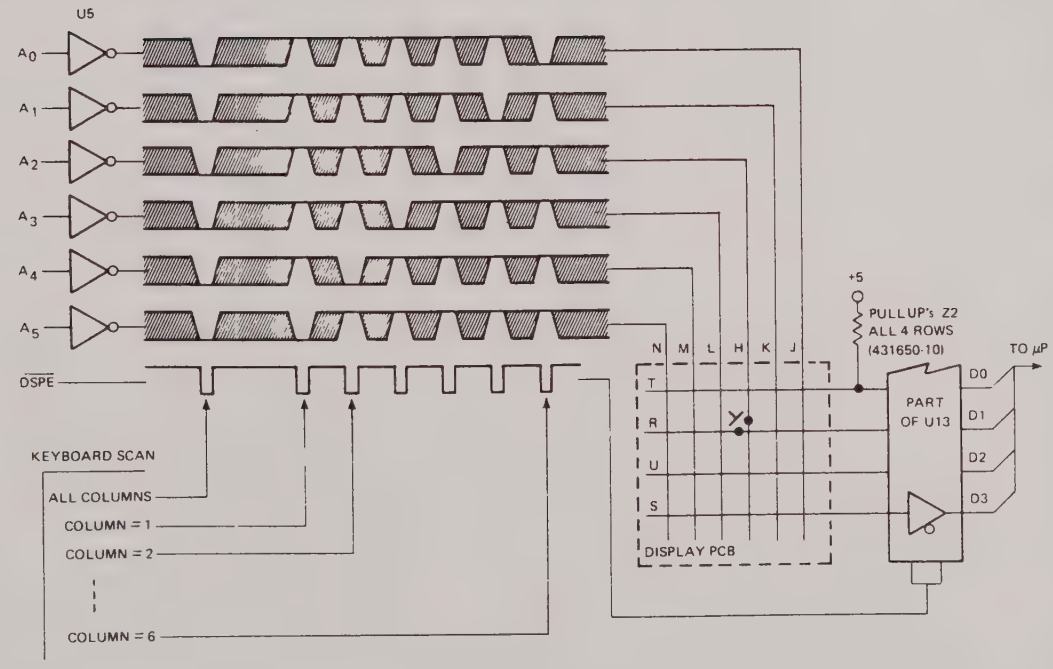

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Figure 3-16. Keyboard Block and Timing Diagram

microprocessor will read a zero on one of the row outputs through U13, the remaining rows will read ones. When a zero does appear, the microprocessor then scans each keyboard column one-at-a-time by reading from U13 with only one of the lines A0-A5 high and others low, until the proper column has been driven low, and that a zero once again appears in the read from U13. Once this occurs, the microprocessor suspends further keyboard scanning and processes the key in software.

3-27. DISPLAY BOARD.

3-28. Display Hardware. The display hardware is configured on the motherboard (MB) as well as on the display board (Dspe). The LSI Display Controller and Driver MB-U12 with the 6-bit Range Latch MB-U1 are located on the motherboard. The display PCB contains the 7-segment LED read-outs DS1 through DS7, buffer drivers Dspe U1, U2 and U3. Function-Range-Status LEDs, and brightness-control current-limiting resistors. This group occupies section 5 on the chassis.

3-29. Display Description. The front panel LEDs are controlled by MB-U12 and MB-U1 through the microprocessor. MB-U1 is a 6-bit latch which is loaded from the data bus by the microprocessor. The outputs of MB-U1 drive 5 range annunciator LEDs and the 'REF' LED. The display configuration is presented in the block diagram figure 3-17. This drawing merges the motherboard and display board components to give an overview of the display schematics 431651 and the display control schematic 431650 (Section 6).

The display device MB-U12 is an LSI display controller with digit and segment drivers that execute the microprocessor's LED bit pattern strobed through the multiplex scan circuitry.

Dspe-U1 is a current sourcing driver which is used to buffer the display controller's column driver in the digit scan sequence. Dspe U2/U3 with associated resistors are current-sinking row drivers. The resistors R1 to R8 set the brightness level of the 7-segment and annunciator LEDs.

3-30. Operation. The display controller shares a chip-select signal with the keyboard hardware. The AY2 output from the microprocessor's address decoder U14 is effectively ORed with the microprocessor's clock via pins U7-5/6 and pins U6-8/9/10, the resulting signal is called $\overline{\text{DSPE}}$. This chip select is supplied as the negative read strobe to the keyboard and the negative write strobe to the display controller.

Whenever the microprocessor wishes to update the LED pattern controlled by MB-U12, it latches a string of bytes into MB-U12 from the microprocessor's address bus. The first of these is a status byte which notifies the display controller that 8 data bytes will follow. The display controller differentiates between status bytes and data bytes by sampling the A8 address line during each write cycle (U12-9), which is high during status bytes and low during data byte writes. See figure 3-18 for a simplified timing diagram.

After all 8 data bytes have been latched into the display controller, it begins to refresh the 7-segment and annunciator LEDs. To do this, the display controller first supplies an excitation MUX pattern to its row driver outputs a-g, which are buffered by DSPE U2/U3 and appear at the cathodes of all LEDs. The display controller then turns on one column driver which, after being buffered by DSPE-U1,

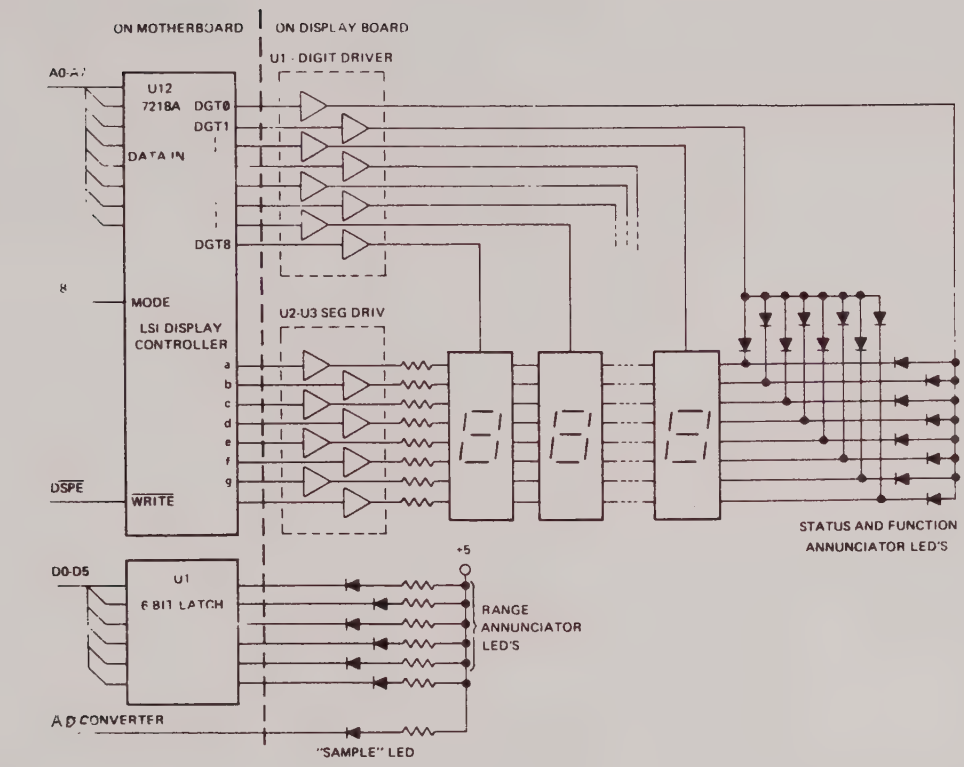

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Figure 3-17. LED Display Hardware

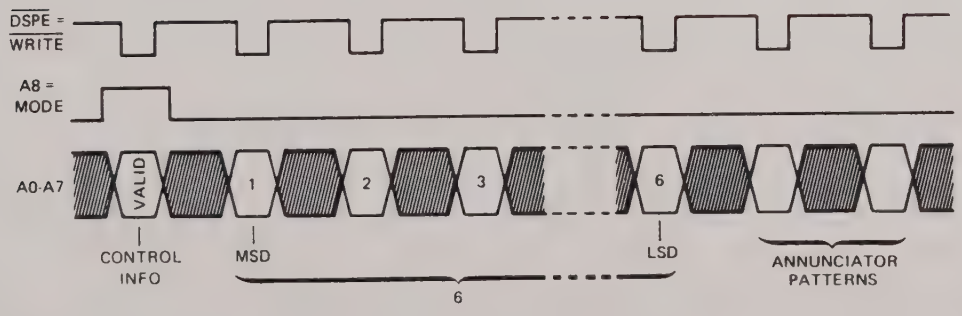

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Figure 3-18. Microprocessor Storage to LSI Display Controller Timing Signals

lights the appropriate LEDs in that column. After a fraction of a millisecond, the controller turns off the column driver, changes the row excitation pattern, and turns on the next column driver, and so on. The LED refresh rate is fast enough that the human eye cannot detect the flicker.

The "Sample" LED located at the lower left corner of the decimal display is not controlled by U12 but instead, receives its control from the analog side of the instrument via OCI-1-10 on drawing 431650-7 (Section 6).

The brightness level for the Range LED's is set by the resistor network Z2.

3-31. GPIB INTERFACE: THEORY OF OPERATION. The DMM's IEEE-488 interface is centered around U44, the 68488 GPIA and positioned in section 7 on the motherboard. The other interface hardware in the GPIB Interface system includes U46 and U47 bi-directional buffer/drivers; U37, U38, and U39 the Serial Poll Disable decoder; U45 the GPIA address switch buffer; U40, U41 and U39 GPIA output holdoff circuit, and U41 the bilateral quad analog switch. These devices provide talker/listener capabilities, most interface commands, and handle serial poll status bytes.

The GPIA interfaces to the bus via U46 and U47 which are bidirectional octal GPIB transceivers. The U46/U47 data direction signal is controlled by the GPIA transmit/receive (T/R2) signal, from pin U44-27. The GPIA interfaces to the microprocessor through 14 registers inside the GPIA which are accessed over the microprocessor's data bus via GPIA pins U44-7 through U44-14.

The microprocessor's address and read/write lines are connected to the GPIA pins 37, 38, 39 and 5 to allow selection of the appropriate internal register by the microprocessor. If the microprocessor reads from the GPIA's register 4, the GPIA will not output data to the microprocessor and will instead drive pin U44-4 low momentarily which will cause U45 to output the address switch setting to the microprocessor.

The GPIA handshakes most in-coming interface messages from the controller and acts upon them without disturbing the microprocessor. If and when an incoming message or data byte requires a response from the microprocessor, the GPIA drives its pin U44-40 low which sends an interrupt request IRQ to the microprocessor via the interrupt control gate U6, discussed in paragraph 3-21. The microprocessor then examines the GPIA's internal registers to release the IRQ and to determine the cause of the interrupt. The same interrupt sequence takes place if the GPIA is made a talker and has no byte to output.

The GPIB "Output Holdoff Circuit" was added between GPIA pin U44-18 and transceiver pin U47-7 to allow the microprocessor more complete control to out-going bytes. This holdoff circuit has no effect except when the DMM is a talker, at which time it is used to hold off the outputting of data and serial poll status bytes.

The GPIB Output Holdoff Circuit contains a 2-bit latch U40. The upper half of U40 is used to affect the output of all bytes while the lower half of U40 is dedicated to controlling the output of serial poll status bytes. U41 is a quad analog switch connected to U39 so that U40 is either enabling the passage of signals between pin U44-18 and pin U47-7 or U41 is forcing a zero on pin U44-8 to make the GPIA believe that no other 488-bus devices are ready for data.

The ICs U37, U38, and U39 pins 3 to 6 are used to decode the interface message "SPD" (Serial Poll Disable = hex 18) but since data on the bus is inverted, the logic must decode the complement of the SPD message. The output from this logic is OR'd with the single line GPIB message IFC (interface clear), inverted and supplied as the reset input to pin U40-13 so that pin U40-8 will be set back to its normal high state after a serial poll has been completed.

3-32. INTERFACE ASSEMBLY THEORY OF OPERATION. Theory of operation of the interface assembly is presented in the following paragraphs; refer to the schematic diagram in figure 6-10 and interconnection diagram figure 6-9.

3-33. Interface DC Power Supply. The interface assembly contains a dual output DC power supply model XM15-5. A schematic diagram of the power supply is shown in figure 6-14. Both sections of the power supply are identical in design but have separate outputs rated for 5 Vdc at 1.5 amperes. Outputs "A" and "B" of the power supply are used to drive the integrated and optical isolator circuits on the interface printed circuit board.

3-34. Interface PCB Theory of Operation. Input signals from the F-111 test station are routed from connector J3 to the optical coupled isolators U10, 11, 20, 21, 26, 27, 35, and 36. The common terminal T is a -12V supply from the test station. The presence of a signal is indicated by illumination of the appropriate LED. The signals are monitored by the microprocessor U32 under control of the Eraseable Programmable Read Only Memory (EPROM) U6 through multiplexers U8, 18, 33, and U40. Following verification of the validity of the commands, the commands are translated by the microprocessor to the appropriate IEEE-488 statements and stored in the RAM section of U46. These are subsequently sent by the microprocessor one byte at a time, through the I/O section of U46 to the IEEE-488 bus interface of U47, 48, 53, and U54. Following receipt of the commands on the IEEE-488 bus, the Racal Dana DMM takes the appropriate measurement and sends the resulting data back to the interface over the IEEE-488 bus. The IEEE-488 data is stored by the microprocessor U32 in the RAM section of U46. The data is then manipulated by the microprocessor by an ASCII to BCD conversion and then sent out to shift registers U4, 15, 44, and U52. The trigger for the shift registers is generated by the microprocessor U32 and logic gates U31. Data from the shift register is buffered by U3, 14, 43, and U51 to optical coupled isolators U1, 2, 12, 13, 22, 41, 42, 37, 49, and U50. These optical isolators provide ground isolation between the microprocessor and the F-111 test station. Status of the output data is monitored by an LED in each line. Power for the floating side of each optical isolator is provided by the isolated 5 Vdc power supply "A". Following shifting out of the data to the test station, the microprocessor sends a status message, PRINT, POLARITY, ERROR, or OVERRANGE, through buffers U43 and U14 and optical isolators U28 and U29.

3-35. Power-up reset circuit. The power-up reset circuit consists of an oscillator and one shot multivibrator that provides a continuous reset until the interface is running correctly.

3-36. Program Description. The microprocessor program is divided into three major functions: self-test, error, and mainline The self-test section performs a test of the major hardware components of the PC board every time the board is either supplied power or reset. The error section deals with the management of errors which occur during the execution of the program. All of the conversion of test station data to and from the Racal Dana DMM is accomplished by the mainline.

3-37. Self-Test. The self-test capability of the program allows for testing of each RAM location, every I/O port of U46, the IEEE-488 bus lines and drivers, the input line multiplexers, and every output line. The RAM check is completed every time the program executes program line '1' (caused by turn on or reset). The integrity of the RAM is verified by writing and then reading back every number between 0 and 256 to each RAM location. Failure of this test is indicated by the number 00041 appearing on the board display. Following the successful completion of the RAM check (but only if the ZERO OHM switch is depressed), the output lines are tested by individually sequencing the output LEDs for a visual check of the operation. The range and function inputs are then read into the processor and any lines which contain a fault are indicated by a corresponding error number. The presence of an input signal during this test will generate an error on that line. Provided that the IEEE-488 bus connector has been removed from the Racal Dana DMM, the bus lines are checked by writing to the bus and then reading back the data. The output display will indicate which if any of the lines are faulty. This also provides a test for the RAM I/O ports and the line multiplexers.

3-38. Mainline Program. The mainline program begins at PGM RUN and reads in the range and function values from the F-111 test station. A routine provides a "soft" debounce for the inputs relays and looks for a track or rebalance signal. If a track or rebalance is found, the front panel switch buttons are "locked out" and can no longer control the Racal Dana DMM. The range and function inputs point to a particular ASCII character string, in a table within the PROM, which contains all of the DMM instructions. This character string is issued to the DMM by the INTRO and HNDSHK subroutines. After the DMM is set up, a delay is initiated whose length is contingent on the time required for the DMM to balance. Once this delay is simulated, the trigger message is sent and the DMM takes a reading. The DMM then issues a service request (SRQ) signal that return data is ready. This is serviced by the SRQSR routine and the measured data is sent to the interface and stored in RAM location MSRMNT. This data is then messaged by the EXPFMT routine which shifts the decimal point of the data until the expected exponent matches that which was returned. The data is then output to output line drivers and the program jumps back to PGMRUN. While the program waits for a new rebalance or track signal, the front keyboard is "unlocked" to allow manual control of the instrument. If the input is in track mode and the measurement is KOHM, a calibration message is sent to the DMM if the ZERO OHMS button is depressed.

3-39. Error Routine. The error routine's primary function is to display and deal with errors which arise during the course of the program. These errors generally call for a rereading of the input signals. For this reason, all errors (with the exception of no range found and overrange) call for a rebalance command from the error routine. When an error occurs, the error number is stored in the D register and the error routine is called. The error routine recalls 'D', outputs 'D', and then issues print and error signals to the test station. After the print pulse is sent, the program enters a loop looking for a rebalance. When rebalance is found, the program jumps to PGMRUN.

SECTION 4

OPERATION

4-1. INTRODUCTION. This section contains operating information for the DMM and Interface. The information contains illustrations of all front and rear panel controls, indicators, and connectors with tabular listing of the function and purpose for each. Operating instructions for manual or bench operation are presented in two ways; a description of each operating feature followed where necessary, by a step-by-step operating example. Some operating features or functions are simple one- or two-step operations and thus no operating examples are included.

Remote operation via the IEEE-STD-488-1978 General Purpose Interface Bus is one of the principal features of the DMM. This section presents bus address selection information and a tabular listing of the device-dependent messages used to program the instrument. Also included is a GPIB program, measurement, and data transfer example.

CAUTION

This instrument may be damaged if operated on line voltage other than that called for by the line VOLTAGE SELECTION viewing window on the rear panel of the DMM.

WARNING

Removal of covers exposes potentially lethal voltages. Do not contact with internal electrical connections while unit is connected to AC power source.

4-2. OPERATION. Before operating the instrument, it is strongly recommended that the operator read this entire section in order to avoid damage to the unit. After reading the operating instructions, refer to the installation section, remove the DMM interface cover, then check the position of the line VOLTAGE SELECTOR through the viewing window on the rear panel of the DMM.

After ensuring that the line VOLTAGE SELECTION is the proper value and the cover on the instrument replaced, connect the power cord to the AC outlet and turn power on the DMM (see section 2-5). Verify that the DMM displays "5005" during the first few seconds after applying power and that the DMM annunciators for "...V" and "AUTO" are ON within a few seconds after applying power.

4-3. CONTROLS AND INDICATORS. The front panel keyboard switches execute all the functions and modes of operation when the DMM is not under Remote (GPIB) control.

The panel designators, keyboard switches (referred to as key), and locations for all controls, indicators, and connectors are illustrated on figures 4-1 and 4-2. The description for each are itemized in tables 4-1 and 4-2.

Table 4-1. DMM Front Panel Controls and Connectors

REFERENCE	ITEM/POSITION	FUNCTION
(15)	☐ ⎓ V Keyboard Switch	Selects the DC volts function, returns the DMM to Internal Reference, enables continuous reading and the AUTO range mode.
(17)	☐ ~V Keyboard Switch	Selects the AC volts function, returns the DMM to Internal Reference, enables continuous reading and enables the AUTO range mode.
(19)	☐ KΩ Keyboard Switch	Selects the resistance measurement function (display reading in kilohms), returns the DMM to internal reference, enables continuous reading and enables AUTO range mode.
(21)	☐ FILTER Keyboard Switch	Enables and disables the 3-pole active filter.
(23)	☐ RESOL Keyboard Switch	Selects the 5 1/2 digit or 4 1/2 digit mode, changing the DMM resolution and read rate.
(25)	☐ AUTO Keyboard Switch	Enables and disables the automatic range mode in all functions.
(26)	INPUT-HI Banana Jack Connector	Serves as the front panel input connector for DC volts, AC volts and resistance measurements.
(27)	EXT REF HI Banana Jack Connector	Front panel input connector for DCV, ACV or KΩ external reference signals.
(28)	EXT REF LO Banana Jack Connector	Front panel input connector for DCV, ACV or KΩ external reference signals.
(29)	⚠	Caution Symbol. Refer to instruction manual for proper use.
(30)	INPUT LO Banana Jack Connector	Front panel input connector for AC volts, DC volts, and for resistance measurements.
(31)	GUARD Banana Jack Connector	Front panel connector to the guard shield of the DMM.
(32)	☐ NULL Keyboard Switch	Enables and disables the NULL function. When enabled, the number in the display is stored as the NULL constant and then subtracted from all future readings until NULL is disabled.

Table 4-1. DMM Front Panel Controls and Connectors (Continued)

REFERENCE	ITEM/POSITION	FUNCTION
(1)	Sample LED	LED Blinks as instrument takes a reading.
(2)	SRQ Annunciator	Indicates that the instrument is transmitting a service request (interrupt) to the controller in systems operation.
(3)	SIGN Annunciator	Displays the – (negative) polarity sign of the mantissa appearing on the display.
(4)	TALK Annunciator	Indicates that the instrument is programmed by the controller to function as a talker on the General Purpose Interface Bus.
(5)	LISTEN Annunciator	Indicates that the instrument is programmed by the controller to function as a listener on the General Purpose Interface Bus.
(6)	REM Annunciator	Indicates that the controller has placed the instrument in the remote operation mode.
(7)	7-Segment Display LEDs	These LEDs display the value of the input signal with appropriate decimal point. They are also used to display constants and function symbols.
(8)	Calibration Switch	Instrument calibration switch recessed behind front panel. Employed only during calibration. Refer to Section 5 for complete instructions.
(9)	⎓ V Annunciator	Indicates that the instrument is in the DC volt function.
(10)	~V Annunciator	Indicates that the instrument is in the AC volt function.
(11)	KΩ Annunciator	Indicates that the instrument is in the kilo-ohms function. The display numbers are expressed in Kohms.
(12)	FILTER Annunciator	Indicates that the 3-pole active filter is enabled.
(13)	AUTO Annunciator	Indicates that the automatic ranging feature (Autorange) is enabled.
(14) (16) (18) (20) (22) (24)	□ RANGE Select Keyboard Switches	Disables autorange and forces the DMM to the selected range.

Table 4-1. DMM Front Panel Controls and Connectors (Continued)

REFERENCE	ITEM/POSITION	FUNCTION
(33)	☐ TRACK Keyboard Switch	Enables the internal trigger and activates continuous readings..
(34)	☐ SINGLE Keyboard Switch	Places the instrument in the HOLD mode and triggers a single reading.
(35)	☐ LOCAL Keyboard Switch	When LOCAL switch is not disabled by the controller, depressing it will return the DMM to local control and display the instrument GPIB address on the 7-segment display.
(36)	☐ RESET Keyboard Switch	Reset returns the DMM to internal reference, internal trigger (continuous readings), and disables NULL.
(37)	☐ REF Keyboard Switch	Enables and disables the external reference selection mode. When enabled, "REF" is displayed on the front panel read-out. Refer to Section 4-11 for complete procedure
(38) (39) (40) (41) (43) (45)	☐ RANGE Select Annunciators	Illuminated LED indicates the DMM's present range setting.
(42)	NULL Annunciator	LED indicates that the NULL feature is enabled.
(44)	EXT REF Annunciator	LED indicates that an external reference is selected.
(46)	POWER Switch-Indicator	Applies AC power to the instrument and initializes the following sequence: a. Performs the AUTO-ZERO test. b. Sets the DMM to internal reference, DCV, Autorange and continuous reading.

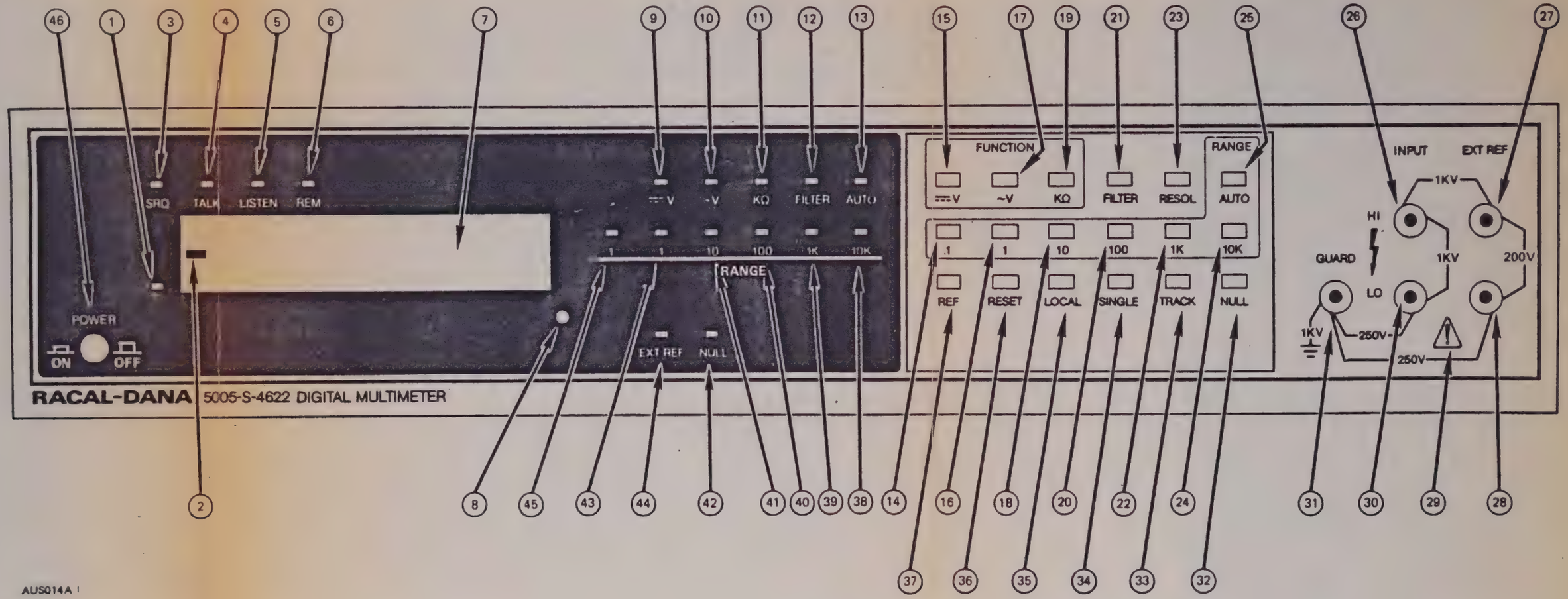

Figure 4-1. DMM Front Panel Controls and Indicators

Table 4-2. DMM Rear Panel Connectors

REFERENCE	ITEM/POSITION	FUNCTION
(1)	EXT. REF. HI-INPUT Banana Jack Connector	Ext. Ref. Hi Input connector parallels front panel connector 27.
(2)	INPUT-HI Banana Jack Connector	HI INPUT connector parallels front panel connector 26.
(3)	SYNCH SIGNAL OUTPUT BNC Connector	Provides negative going TTL pulse each time that a reading is displayed. Used to synchronize input signal scanners such as Racal-Dana Model 1200 or printers. See Section 4-15 for more details.
(4)	FUSE HOLDER	Primary powerline fuse. Use 1/2 amp slo-blow for 110-120V operation or 1/4 amp slo-blow fuse for 220-240 volt operation.
(5)	AC POWER CONNECTOR	Three wire connector plug for AC power line load.
(6)	GPIB ADDRESS SWITCHES	Allows selection of "Talk Only" mode as well as selection of DMM's GPIB address which identifies the DMM in systems operation.
(7)	GPIB CONNECTOR IEEE-STD-488 PORT	General Purpose Interface Bus. This connector is configured in accordance with the IEEE 488-1978 standard interface.
(8)	EXT. TRIG. INPUT BNC Connector	Provides an input to allow the triggering of readings by a negative-going TTL pulse. See Section 4-14 for further details.
(9)	GUARD Banana Jack Connector	Provides rear panel connector for the guard shield in the DMM. Parallels front panel connector 31.
(10)	INPUT-LO Banana Jack Connector	Low input signal connector parallels front panel connector 30.
(11)	EXT. REF. LO INPUT Banana Jack Connector	Ext. Ref. Lo Input connector parallels front panel connector 28.

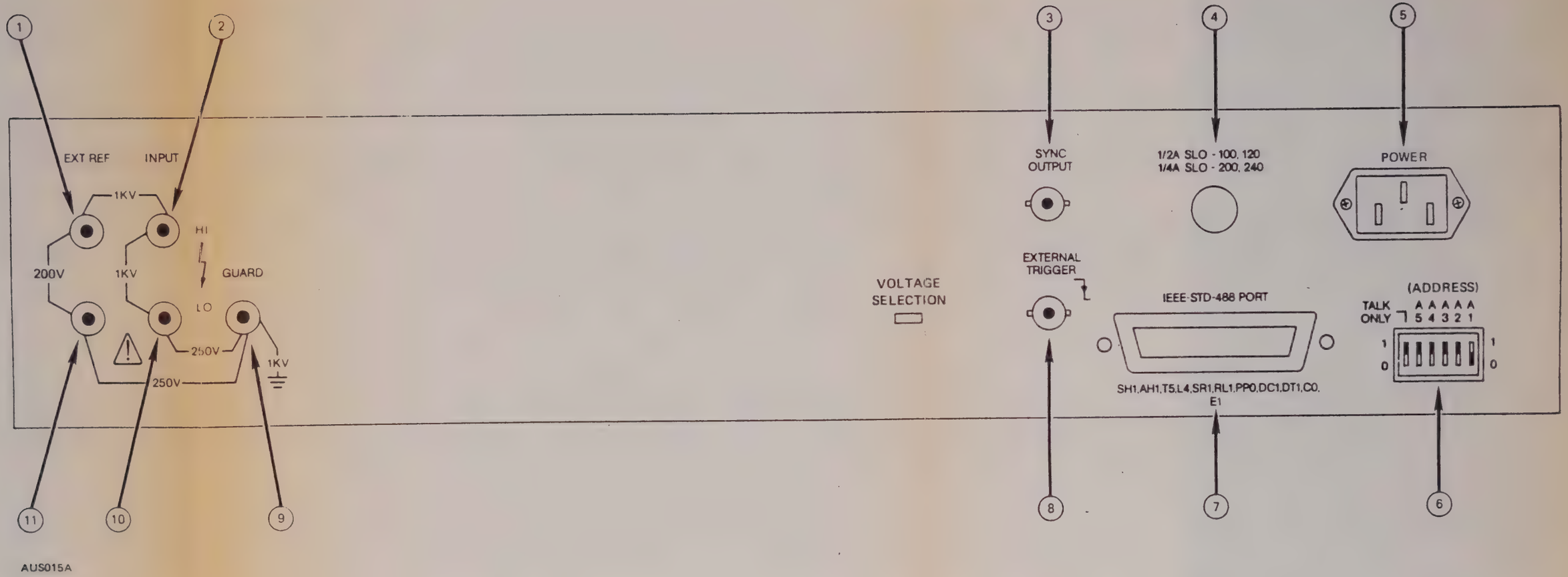

Figure 4-2. DMM Rear Panel Connectors

Table 4-3. Interface Front Panel Controls and Connectors

REFERENCE	ITEM/POSITION	FUNCTION
1	ON-OFF Switch	Controls primary power to both the DMM and the Interface.
2	ZERO OHM Switch	Is active when the DMM is under the control of the AGERD and in Kohm and TRACK modes. When depressed, the resistance path is measured and the value subtracted from all subsequent ohms readings. NOTE: This operation requires that a short be installed at the DMM input terminals. Some test programs provide this short at the ITA to account for wiring and relay contact resistance.
3	NORMAL-TRACK-REBAL Switch	In NORMAL position, the DMM is under control of the AGERD. On station command, a reading will be initiated by the DMM. In TRACK position, the TRACK switch on the Racal-Dana DMM must be depressed to initiate tracking capabilities. The REBAL is a momentary position and initiates a new reading. It can also be used to clear error conditions following an unsuccessful reading. Any such errors are indicated by the ERROR light or DMM BAL on DATAC. It will also provide a PRINT signal when the DMM is in the TRACK mode.
4	J6 Connector	Is parallel connected with J1 (rear panel) to provide front panel access to DMM Ratio Measurement.

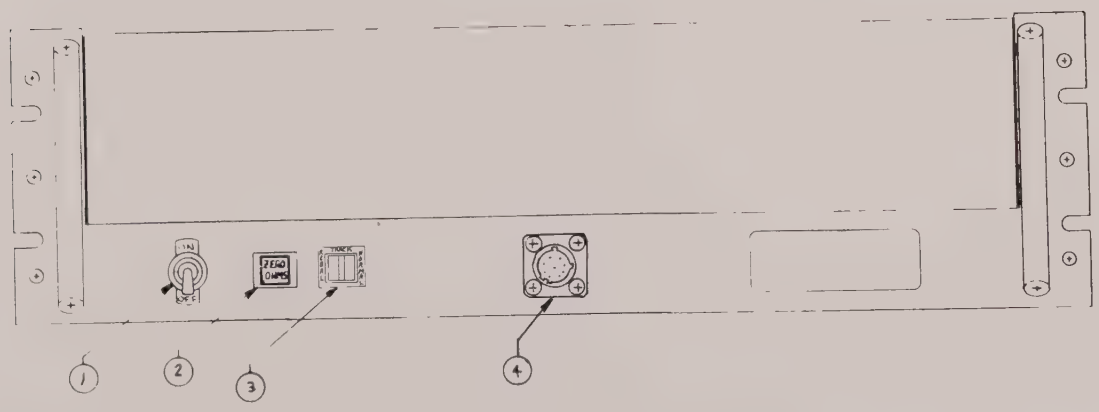

Figure 4-3. Interface Front Panel Controls and Connector

Table 4-4. Interface Rear Panel Connectors

REFERENCE	ITEM/POSITION	FUNCTION
1	J3	Connects DMM Interface board to F-111 Test Set
2	J1	Provides connection for DMM Ratio measurement. Is parallel connected to J6 (front panel).
3	J4	Connects DMM Interface board to F-111 Test Set
4	J2	AC Power Input. Provides connection for 115 vac, 60 Hz.

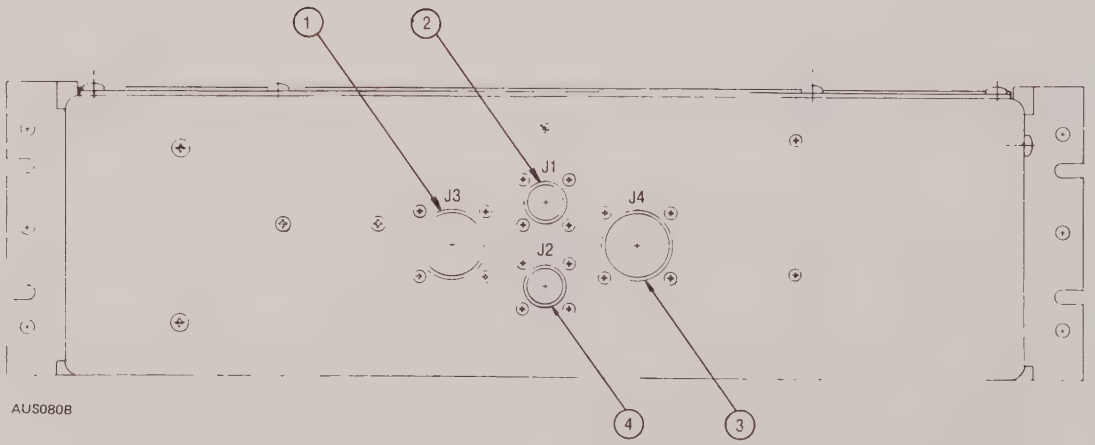

Figure 4-4. Interface Rear Panel Connectors

4-4. BASIC MEASUREMENTS.

4-5. Zero Command. After the DMM is initialized by power-on and at other selected intervals after turn-on, the Zero Command should be performed. This procedure assures that the DMM readings remain within specifications as it approaches normal operating temperature. The Zero Command operation is performed as described in the following steps:

a. Short the HI-LO INPUT terminals.

b. Select the DCV function. Depress and hold the .1 range key (.1 LED indicator glows) until the display read-out displays "CAL 0" verifying that zero command was enabled. Release the .1 DCV key.

c. This procedure corrects the Isolator and Digitizer offset.

4-6. Range Control. Upon initialization, the DMM goes to its home state; autorange and continuous readings. With a signal applied to the INPUT HI-LO terminals, AUTO range will set the range to match whatever signal the DMM sees at the input terminals. For example, if a 6 volt battery is connected to the input terminals and the DMM is initialized by power turn-on, the DMM goes through the auto-test routine and AUTO range will select the 10 volt range.

To manually disable AUTO range, depress one of the range switches once. This action extinguishes the AUTO range annunciator and the DMM will now respond to the selected range.

4-7. DC Volts Measurements. The basic instrument is capable of measuring DC volts in 5 ranges: 0.1V, 1V, 10V, 100V, 1000V. To measure DC voltage proceed as follows:

a. Connect the instrument to the primary AC power source, turn the power switch on and allow it to initialize. Verify that the DMM initializes as described in paragraph 4-2.

b. Connect the DC voltage to the INPUT HI-LO terminals, refer to figures 4-5 and 4-6, and read the value from the display and range annunciators.

4-8. AC Volts Measurements. The DMM is capable of measuring AC volts in 4 ranges: 1V, 10V, 100V, 1000V. To measure AC voltage proceed as follows:

a. Connect the DMM to the primary AC power source, turn the power switch on and allow it to initialize. Verify that the DMM initializes as described in paragraph 4-2.

b. Select the AC volts function by pressing the AC key, then verify that the AC annunciator LED is on.

c. Connect the AC voltage to the INPUT HI-LO terminals, refer to figures 4-5 and 4-6, and read the value from the display and range annunciators.

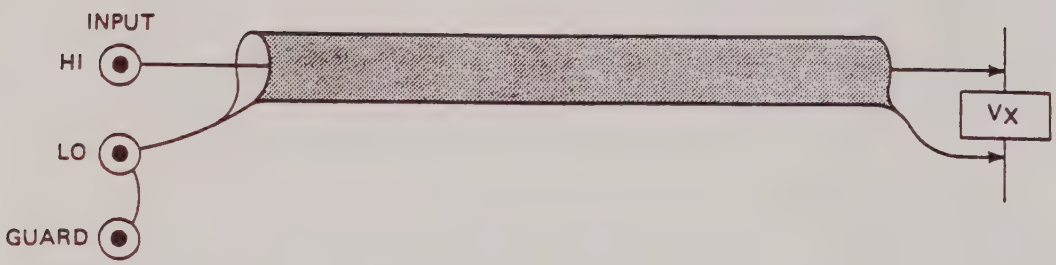

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Figure 4-5. DC, AC Measurement Connections Using Coaxial Cable

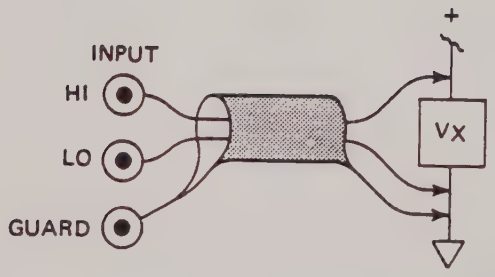

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Figure 4-6. DC, AC Measurement Connection Using Two-Conductor Shielded Cable

4-9. Resistance Measurement. The DMM is capable of measuring resistance values in six Kohm ranges: 0.1K, 1K, 10K, 100K, 1000K, 10,000K. To measure resistance proceed as follows:

a. Connect the instrument to the primary AC power source, turn the power switch on and allow it to initialize. Verify that the DMM initializes as described in paragraph 4-2.

b. Select the resistance function by pressing the KΩ key and verify that the KΩ annunciator LED is on.

c. Connections for a simple shielded ohms measurement are shown in figure 4-7. The drawing consists of a single-conductor shielded cable connected between the unknown resistance Rx and the 5005's front panel or rear panel signal input connectors. While reasonably accurate measurements can be made with this method, cable resistance reduces accuracy when measuring medium to low value resistances.

d. In high noise-level environments, the configuration shown in figure 4-8 is recommended. The input terminals are connected to the unknown resistance either by a 2-conductor shielded cable or 2 separate coaxial cables. In either case the shields are connected to GUARD to help increase noise immunity.

e. When the lead resistance begins to affect measurement accuracy, the following procedure can be used. When the measurement cable is short this procedure may be necessary in the .1K and possibly the 1K ohms range. When operating in an automated measurement system, the unknown resistance may be connected to the DMM by long lengths of wire, then the following measurement procedure is suggested on the 0.1K through 10K ohms ranges to cancel the lead resistance offset.

4-10. Lead Resistance Nulling Procedure:

a. Select the ohms function and 0.1KΩ range.

b. Connect the measurement leads to the input connectors on the Model 5005.

c. Examine the NULL annunciator to determine if NULL is already enabled. If so, disable NULL by pressing the NULL keyswitch.

d. Short the measurement lead together at the point of measurement.

e. If the instrument is in the HOLD mode, trigger 1 or more readings by pressing SINGLE or TRACK.

f. Press the NULL keyswitch. This will cause the 5005 to store the previously measured lead resistance as the NULL constant and subtract it from future readings.

g. Remember to disable the NULL function when ohms measurements have been completed.

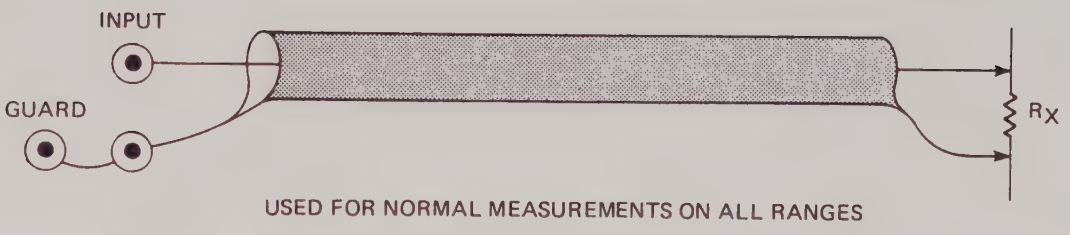

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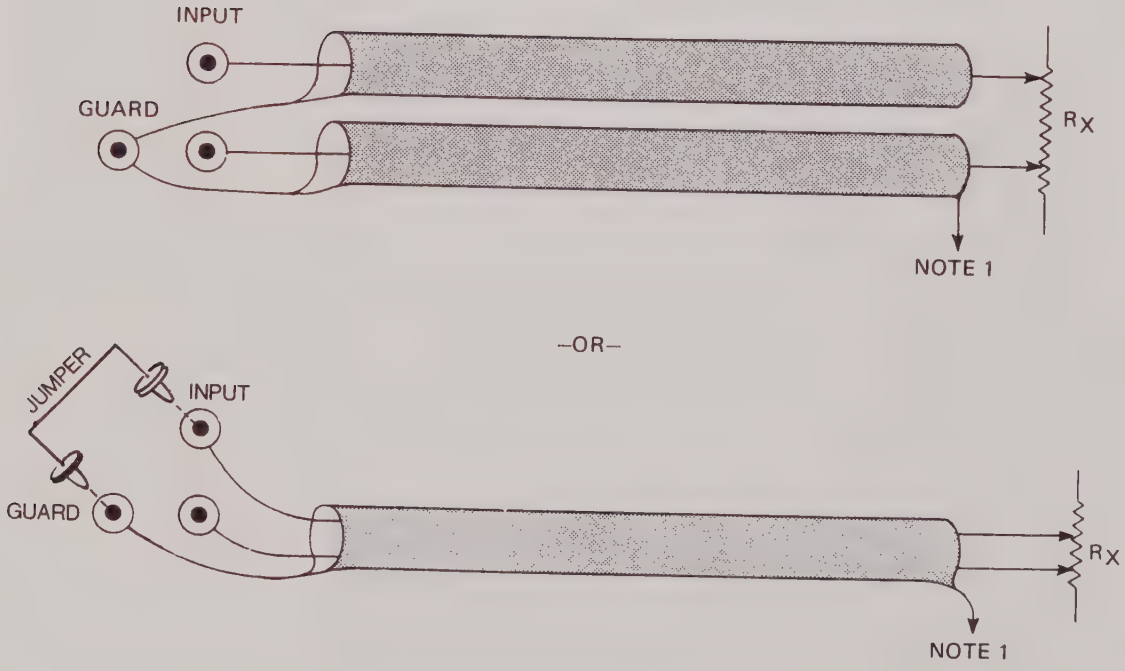
Figure 4-7. Simple Shielded Ohms Measurement Connection



NOTE 1: LEAVE OUTER END OF SHIELD FLOATING OR CONNECT TO SHIELDS AS REQUIRED
2: INSTALL JUMPER FOR DC VOLTAGES TEST –28V TO +160V, AC FROM 62 MV TO 115V @ 400 HZ, 115V 60 HZ, AND POSITIVE RATIO MEASUREMENTS

AUS030A

Figure 4-8. Connections Used in High Noise Environments

4-11. Ratio (External Reference) Measurements. Ratio measurements are made by applying a DC, AC, or Ohms external reference signal to the DMM's reference input terminal and then selecting the appropriate external reference function and external reference range with the following keyboard procedure. See paragraph 4-22 for a description of the corresponding GPIB program codes.

The 'REF' key enables and disables the external reference selection mode. When the external reference select mode is enabled, "REF" is displayed on the DMM's front panel and the annunciator LEDs display the present reference function and range. If while in the REF select mode all the function LEDs remain blank, this indicates that the DMM's internal reference has been selected.

While in the REF select mode, an external reference function or range can be selected. This is done by pressing a function or range key. The following keys will modify the reference function or range setting:

FUNCTION

V V K

RANGE

.1 1 10 100 1K 10K AUTO

The annunciator LEDs will then indicate the new reference setting.

Once the reference function and range have been selected, the REF key is pressed (to exit the REF Select mode) and the DMM begins taking readings. The "EXT REF" LED will be lit if an external reference function has been selected. When not lit this indicates that the DMM is using its internal reference.

The user can return to Internal Reference by pressing a Function key when not in the REF select mode, or by pressing the RESET key at any time. To examine the Reference setting without disturbing it, press the "REF" key to enter the REF select mode, examine the Function and Range annunciators, and then press "REF" again to exit the REF select mode.

4-12. Error Messages. Error messages are classified in two categories: General Error Messages and GPIB Error Messages. The general error messages with numerics 0 through 9 apply to local and remote operations. GPIB error messages with numerics 10 through 13 apply only to remote operation.

For local operation, the DMM employs the 7-segment display to exhibit the error message code numbers. The error message numbers and explanations are listed in table 4-5.

For remote GPIB operation, the DMM transmits an SRQ to the controller; the controller replies with the "Y" program code to the DMM to request the error message number. The remote error message numbers and explanations are listed in table 4-5. Refer to paragraph 4-46 for further explanation of the "Y" program code.

Table 4-5. General and Remote Error Messages

Error Message No.	Error Message
	GENERAL ERROR MESSAGES
1	Not in the DC function, 0.1 range when zeroing the instrument.
2	Attempting to zero the instrument with an input voltage applied or to be input open-circuited. Connect a short across input terminals and repeat zero command.
3	The microprocessor's on-board RAM is defective (U35 on the motherboard).
4	The contents of the non-volatile memory have been disrupted, therefore the instruments calibration should be verified.
6	Attempted display of a number which is beyond 9.999E9, unlike the other error messages, Error 6 is always displayed on the front panel and never causes an SRQ to be sent to the controller, independent of whether the instrument is in local or remote.
7	The Model 5005 RAM is defective (U31 on the motherboard).
8	An attempt was made to store an overload reading to a register inside the DMM.
	GPIB ERROR MESSAGES
11	Triggered too fast or too often.
12	Syntax error during GPIB programming.

4-13. DMM Pulse Level/Timing Characteristics.

4-14. External Trigger. The signal level and timing requirements for the external trigger are presented in figure 4-9. These timing requirements are not critical when in local control as the DMM interprets a tight group of external triggers as a single trigger command and the rise and fall time specifications stated in figure 4-9 do not apply, due to this internal debouncing. This allows the use of mechanical foot switches and other "noisy" signal sources with good results. When in remote, all external triggers are treated individually and two or more closely spaced triggers will cause the DMM to issue an SRQ to the bus and make an error message available to the controller.

4-15. Sync Output. The DMM provides a synchronizing output pulse from a BNC connector on the rear panel. Refer to figure 4-2. This pulse, timing shown in figure 4-10, indicates when the DMM has finished a reading or a sequence of readings. This output pulse can be used to sequence a signal scanner or other device as shown in figure 4-11.

When Autorange is selected, the sync output will not appear until the DMM has completed autoranging, and has taken the reading on the proper range.

4-16. SYSTEM OPERATION. This subsection presents information on the operation of the 5005 in a system.

4-17. General Purpose Interface Bus. The IEEE-488-1978 (GPIB) Interface provides remote programming for all controls and the output of data from the DMM. Inputs and outputs are made via a 24 pin connector, see figure 4-12, located on the rear panel. The pin location, line identification, and operation of the GPIB are in compliance with IEEE-STD-488-1978. The GPIB provides interface capability with other instruments and with a controller also utilizing the "interface bus" structure. Connector pin assignments are shown in figure 4-13. The IEEE-488-1978 subsets available are listed in table 4-6.

By assigning a unique address to the DMM, it can be "called up" by the controller or another device on the bus without interfering with other units on the bus. Switches located on the rear panel of the DMM permit the programming of the instrument address. The coding used for the address is binary. Any one of 31 codes can be used for the address of an instrument, but a total of 15 is the maximum number of devices that can be used on one bus.

4-18. GPIB Description. Of the 24 lines available at the connector shown in figure 4-12, seven are grounds, one is a shield, and the remaining 16 lines are the signal lines. All of the signal lines are either input or output lines and have the following characteristics:

Logic Levels	1 = Low = .8V 0=Hi= 2.0V
Input Loading	Each input two TTL loads
Output	The output is capable of driving 15 interface bus loads. It consists of an open collector driver and is capable of sinking 48 mA with a maximum voltage drop of 0.5 volt. See IEEE 488 Electrical Specifications.

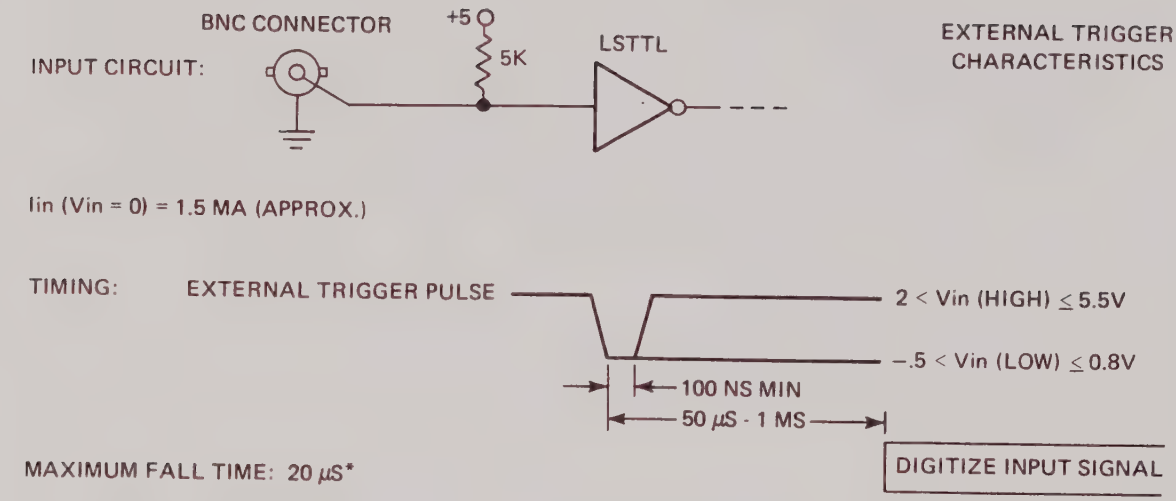


Figure 4-9. External Trigger Characteristics

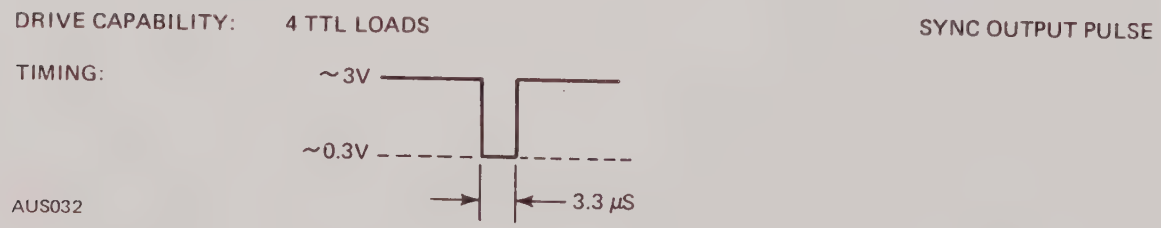


Figure 4-10. Sync Output

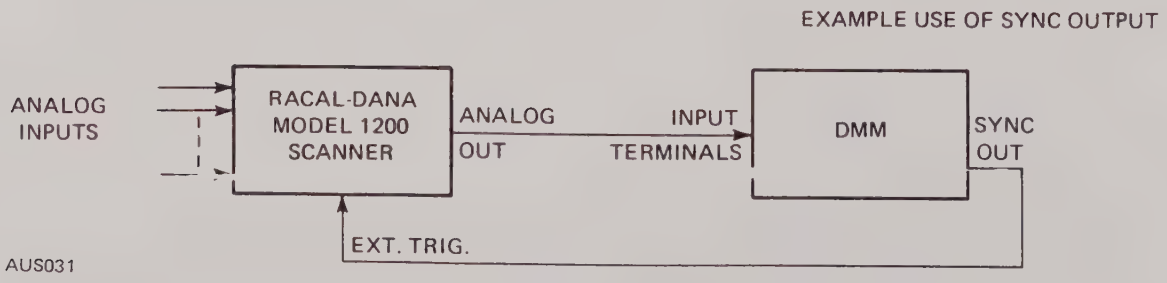


Figure 4-11. Sync Application

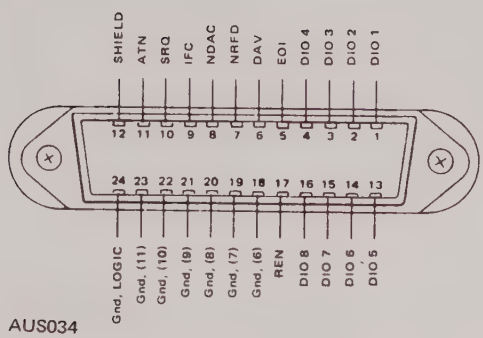
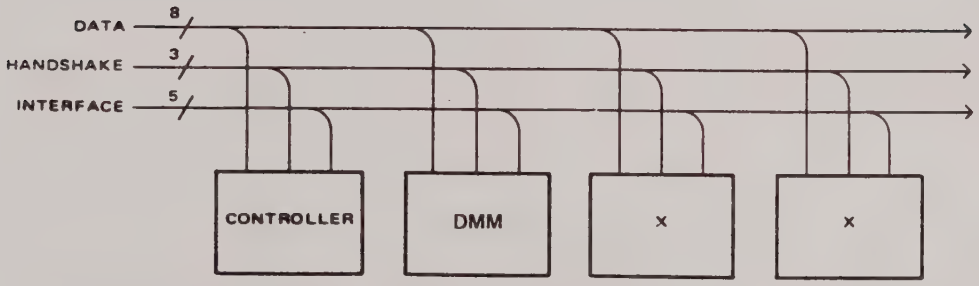


Figure 4-12. GPIB Connector (Rear Panel)



PIN			PIN	
1	DIO-1 Data In/Out Bit 1 (LSB)	DATA LINES ARE USED TO TRANSFER DATA FROM ONE INSTRUMENT TO ANOTHER	12	SHIELD
2	DIO-2 Data In/Out Bit 2		18	GND
3	DIO-3 Data In/Out Bit 3		19	GND
4	DIO-4 Data In/Out Bit 4		20	GND
13	DIO-5 Data In/Out Bit 5		21	GND
14	DIO-6 Data In/Out Bit 6		22	GND
15	DIO-7 Data In/Out Bit 7		23	GND
16	DIO-8 Data In/Out Bit 8		24	LOGIC GND
6	DAV (DATA VALID)	HANDSHAKE LINES OPERATE IN A PROPER TIME SEQUENCE FOR COMPLETE COMMUNICATION BETWEEN INSTRUMENTS	25	NOT USED
7	NRFD (NOT READY FOR DATA)			
8	NDAC (NOT DATA ACCEPTED)			
5	EOI (END OR IDENTIFY)	INTERFACE LINES ARE USED TO PROVIDE AN ORDERLY FLOW OF INFORMATION BETWEEN UNITS		
9	IFC (INTERFACE CLEAR)			
10	SRQ (SERVICE REQUEST)			
11	ATN (ATTENTION)			
17	REN (REMOTE ENABLE)			

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Figure 4-13. Interface Signal Pin Assignments

Table 4-6. IEEE 488-1978 Standard Interface Subset Capability

GPIB Subset	Description	Applicable Capability
SH1	Source Handshake	Complete Capability
AH1	Acceptor Handshake	Complete Capability
T5	Talker	Complete Capability (1) Basic Talker (2) Serial Poll (3) Talk only Mode (4) Unaddress if MLA
TE0	Extended Talker	None
L4	Listener	Complete except Listen Only (1) Basic Listener (2) Unaddress if MTA
LE0	Extended Listener	None
SR1	Service Request	Complete Capability
RL1	Remote/Local	Complete Capability (1) REN - Remote Enable (2) LLO - Local Lockout (3) GTL - Go to Local
PP0	Parallel Poll	No Capability
DC1	Device Clear	Complete Capability (1) DCL - Device Clear (2) SDC - Selected Device Clear
DT1	Device Trigger	Complete Capability GET - Group Execute Trigger
C0	Controller	No Capability
E1	Open Collector Bus Drivers	

The signal lines, as shown in figure 4-13, consist of three functionally separate sets: Data, Handshake, and Interface.

4-19. Data. The data lines consist of lines DIO-1 through DIO-8. These lines are the lines over which data flows between all instruments on the bus in bit parallel, byte serial form.

4-20. Handshake. The transfer lines consist of: DAV (data valid), NDAC (not data accepted), and NRFD (not ready for data). These lines provide communication (between the instrument that is talking and the instruments that are listening) to synchronize the flow of information across the eight data lines. These lines derive their nomenclature from their meaning in the low or one state (e.g., when NRFD is low the device is Not Ready For Data).

a. DAV. Signifies that valid information is available on the data lines.

b. NRFD. Signifies that the instrument is not ready to accept information.

c. NDAC. Signifies that the information is not accepted by the acceptor.

4-21. Interface. Five interface lines coordinate the flow of information on the bus:

a. Interface Clear
'IFC'. Places the DMM interface in the IDLE state.
(Untalk, Unlisten.)

b. Attention
'ATN'. Indicates the nature of information on data lines during a handshake transfer sequence. Low indicates data lines carry interface commands; high indicates that the data lines carry data.

c. Remote Enable
'REN'. Arms instrument to select Remote Operation.
(Low for Remote.)

d. Service Request
'SRQ'. Service request signal line. Signals the controller that a peripheral or bus member wants attention for such purposes as transmitting measurement, status, or condition information to the bus controller.

e. End or Identify
'EOI'. End or Identify signal. Used for two purposes: (1) to signify the end of a message and (2) to signal bus peripherals to set the I/O bit assigned for parallel poll identification process.

4-22. Handshake. The handshake is the process by which each data byte is transferred from the source to the acceptor. Figure 4-14, the handshake flowchart illustrates the sequential relationship between the DAV, NRFD, and NDAC lines used to transfer data bytes.

4-23. Address Assignment. When the DMM is used as a system instrument it must be assigned an address as a bus member. The instrument is equipped with an address switch located on the rear panel which enables the user to assign it one of 31 decimal addresses The decimal addresses available are the numbers 00 through 30.

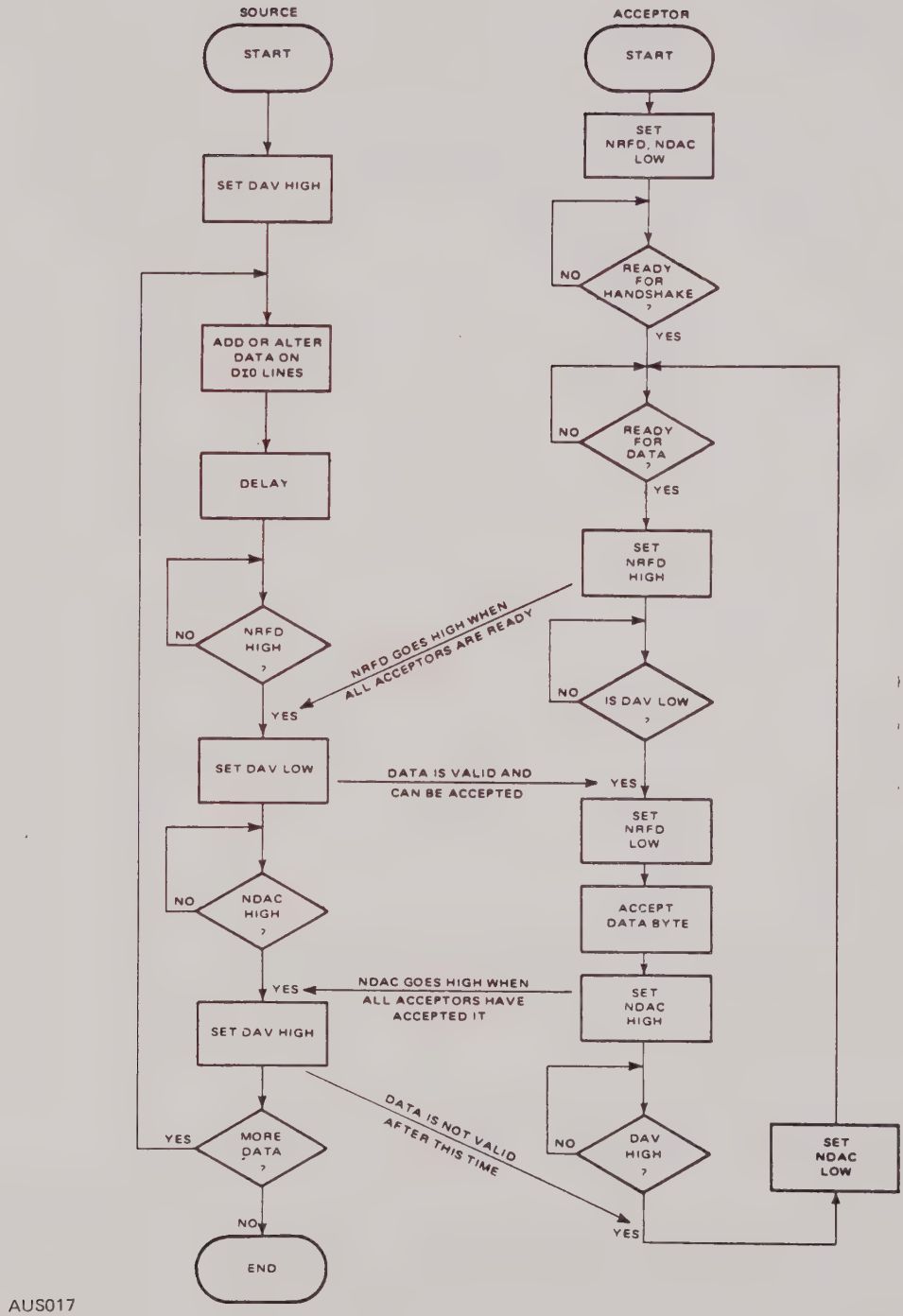

Figure 4-14. Handshake Flow Chart

Table 4-7 contains all of the information required for setting the instrument address switch and for determining the talk and listen address codes used in programming the controller.

Refer to table 4-7 and note that the right hand column shows the decimal addresses available for assignment to the DMM. The column titled Address Switch Setting illustrates the positions of the switches for each decimal address. To set the address on the instrument at the desired decimal address, refer to table 4-7, and set the switches on the address switch to the pattern shown in the Address Switch column of the table.

As an aid in setting the address switches, the decimal address may be displayed on the DMM readout by holding the "Local" key down. The address switches may then be set until the desired address appears on the display. Turning on the "Talk Only" switch will cause the displayed address to be 64 or greater. This illegal address is displayed to alert the user that the DMM is in the "talk only" mode.

Once the instrument has been assigned an address, and the address switch has been set, the controller may address the instrument as a talker or as a listener by transmitting the appropriate ASCII character on the data lines. The Data Lines column shows the 7 bit binary code required for each talk and listen address assigned to the instrument. These are the codes the controller must transmit to establish the talker/listener condition of the DMM. Note that there are two address codes used for each decimal address. Each of these address codes constitutes a different ASCII character. For example, if it is desired to use the decimal address 02, the address switch on the rear panel of the instrument is set to the pattern shown in table 4-7. As shown in the table, the talk address is the ASCII character " and the listen address is the ASCII character B. Note that the only difference in the binary code in each case is the state of data lines D6 and D7.

Table 4-7 illustrates the data line code in binary form for each decimal address. Again, using the example for decimal address 02, note that bits D1 through D5 are the same for both talk and listen address and that the only difference is in bits D6 and D7.

4-24. Bus Operation Sequence. The transmission of programming instructions to the DMM and the subsequent transmission of measurement data to the controller are accomplished by transmitting programming instructions as outlined in the bus operation sequence in table 4-8. Table 4-8 and the accompanying timing chart (figure 4-15) illustrate the sequence of the transmission of device dependent messages to the DMM which cause it to measure the voltage applied to the input and then transmit the resultant measurement data to the controller via the interface bus.

Note that the left hand column of table 4-8 contains line numbers. These are used for reference purposes throughout the following description of the bus operation sequence. The column titled Handshake Lines indicates the high/low condition of the handshake lines at various points throughout the two-way transmission of information. In a similar fashion the columns titled Interface Lines and Data Lines contain entries reflecting the state of the interface lines and data lines during operation. The column titled Meaning or Function contains entries explaining the purpose of each operational step during the data transfer.

Table 4-7. Instrument Address Selector

ASCII CHARACTERS		DATA LINES							ADDRESS* SWITCH SETTING	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1		
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	SP	0	1	0	0	0	0	0		00
@		1	0	0	0	0	0	0		
	!	0	1	0	0	0	0	1		01
A		1	0	0	0	0	0	1		
	"	0	1	0	0	0	1	0		02
B		1	0	0	0	0	1	0		
	#	0	1	0	0	0	1	1		03
C		1	0	0	0	0	1	1		
	$	0	1	0	0	1	0	0		04
D		1	0	0	0	1	0	0		
	%	0	1	0	0	1	0	1		05
E		1	0	0	0	1	0	1		
	&	0	1	0	0	1	1	0		06
F		1	0	0	0	1	1	0		
	' (APOSTROPHE)	0	1	0	0	1	1	1		07
G		1	0	0	0	1	1	1		
	(	0	1	0	1	0	0	0		08
H		1	0	0	1	0	0	0		
	)	0	1	0	1	0	0	1		09
I		1	0	0	1	0	0	1		
	*	0	1	0	1	0	1	0		10
J		1	0	0	1	0	1	0		
	+	0	1	0	1	0	1	1		11
K		1	0	0	1	0	1	1		
	,	0	1	0	1	1	0	0		12
L		1	0	0	1	1	0	0		
	--	0	1	0	1	1	0	1		13
M		1	0	0	1	1	0	1		
	.	0	1	0	1	1	1	0		14
N		1	0	0	1	1	1	0		
	/	0	1	0	1	1	1	1		15
O		1	0	0	1	1	1	1		

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* Switches in the "ON" or logical "1" position are shown in black. Switches in the "OFF" or logical "0" position are shown in grey.

Table 4-7. Instrument Address Selector (Continued)

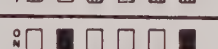
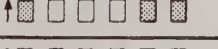
ASCII CHARACTERS		DATA LINES							ADDRESS* SWITCH SETTING	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1		
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	Ø	0	1	1	0	0	0	0		16
P		1	0	1	0	0	0	0		
	1	0	1	1	0	0	0	1		17
Q		1	0	1	0	0	0	1		
	2	0	1	1	0	0	1	0		18
R		1	0	1	0	0	1	0		
	3	0	1	1	0	0	1	1		19
S		1	0	1	0	0	1	1		
	4	0	1	1	0	1	0	0		20
T		1	0	1	0	1	0	0		
	5	0	1	1	0	1	0	1		21
U		1	0	1	0	1	0	1		
	6	0	1	1	0	1	1	0		22
V		1	0	1	0	1	1	0		
	7	0	1	1	0	1	1	1		23
W		1	0	1	0	1	1	1		
	8	0	1	1	1	0	0	0		24
X		1	0	1	1	0	0	0		
	9	0	1	1	1	0	0	1		25
Y		1	0	1	1	0	0	1		
	:	0	1	1	1	0	1	0		26
Z		1	0	1	1	0	1	0		
	;	0	1	1	1	0	1	1		27
[		1	0	1	1	0	1	1		
	<	0	1	1	1	1	0	0		28
\		1	0	1	1	1	0	0		
	=	0	1	1	1	1	0	1		29
]		1	0	1	1	1	0	1		
	>	0	1	1	1	1	1	0		30
^		1	0	1	1	1	1	0		
NONE		ILLEGAL							NONE	31

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Table 4-8. Bus Operation Sequence

	HANDSHAKE LINES	BUS LINES	DATA LINES	MEANING OR FUNCTION
1		REN Lo		Arms bus peripherals to go to remote mode.
2		IFC		Stops activity on the bus.
3		ATN Lo		Signifies that data byte will be a "Bus Message".
4	NRFD Hi			DMM says ready for data.
5			?	UNL (Unlisten) message (ASCII character ?) on data bus by controller means "all bus peripherals unlisten".
6	DAV Lo			Controller says data on bus is valid.
7	NRFD Lo			DMM says its not ready for new data; do not change data lines while DMM is accepting data.
8				DMM reads data lines.
9	NDAC Hi			DMM says it has read data.
10	DAV Hi		?	Controller says data no longer valid.
11	NDAC Lo			DMM removes data accepted flag.
12	NRFD Hi			DMM says it's ready for next data byte.
13				Controller removes or changes data on bus.
14			U	"I talk", controller becomes talker (HP9825 talker address).
15			"	"You listen", addressed peripheral becomes listener (In this case it is the 6000 DMM set to decimal address 02; see table 3.9).
16		ATN Hi		Signifies that data byte will be a "Device Dependent Message" as opposed to an "Interface Message".
17			F	Function
18			1	DC Volts
19			R	Range
20			5	10 Volts
21			T	Trigger
22			1	Continuous
23			CR	End of transmission by HP9825.
24			LF	
25		ATN Lo		Byte to follow is a Bus Message.
26			?	UNL (unlisten) bus message.
27			B	"You talk", DMM talk address (02).
28			5	"I listen", HP9825 listen address.
29		ATN Hi		Message to be transmitted by DVM is Data.
30			+	} Measurement data transmitted by DMM
31			1	
32			.	
33			0	
34			2	
35			5	
36			4	
37			6	
38			8	
39			E	Exponent Indicator means X 10^{01}
40			+	Sign of exponent.
41			0	} Exponent. Here it indicates 10^{10}.
42			1	
43			CR	} End of data message.
44			LF	

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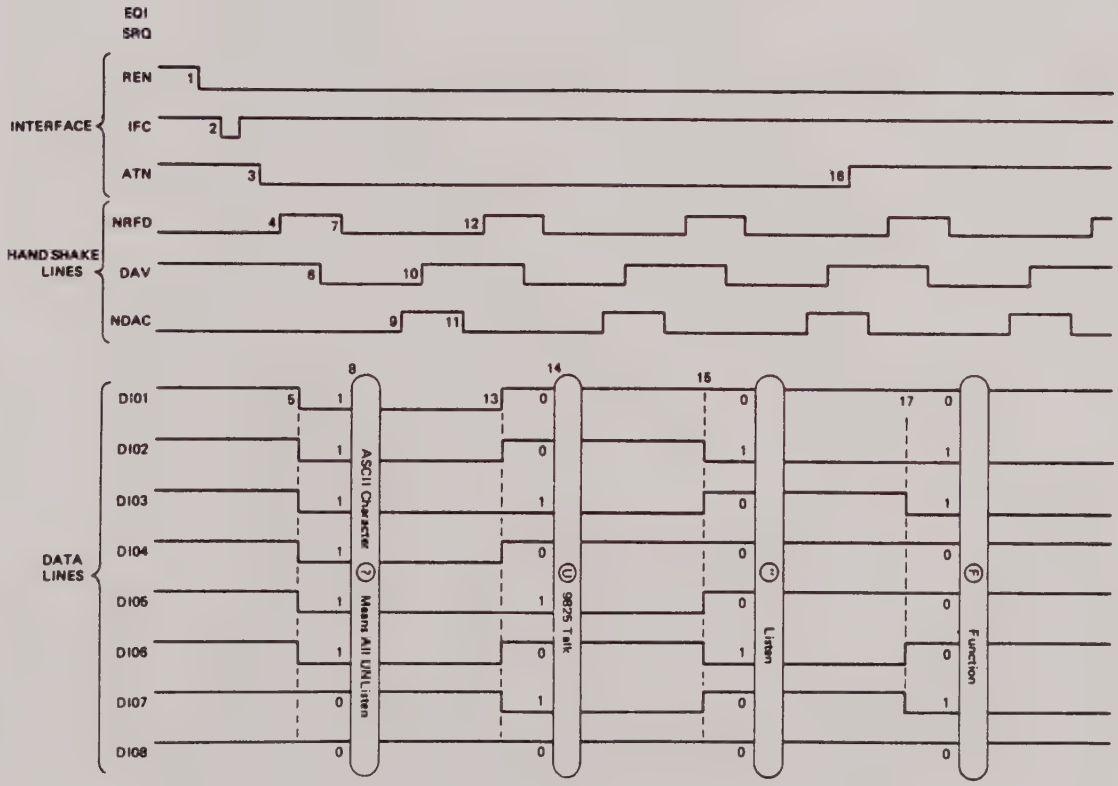

Figure 4-15. Interface Timing

A timing chart is included to illustrate the condition of each individual bus line at each stage of the data transfer operation. Note that the timing chart includes numbers adjacent to each level change. These numbers refer to the individual line entries of the table.

The measurement operation used in table 4-8 is a simple voltage measurement. The measurement parameters are as follows: Function DC volts, Range 10 volts, Trigger continuous. Note that the measurement parameters are shown in the meaning or function column of the table in lines 17 through 22 and that the program string required to perform this measurement is F1R5T1. The program string will include a carriage return and line feed, but in this case this command is automatically transmitted by the Hewlett Packard 9825.

For purposes of this example it is assumed that the DMM has been assigned the decimal address 02 and that the controller is a Hewlett Packard 9825 calculator with a talk address U. It is further assumed that both the controller and the DMM are system connected, turned on, and operational.

Table 4-8 shows the sequence of bus operation. Lines 1 through 13 show the detailed operation of the bus for one handshake cycle (i.e.: the transmission of one ASCII character as a bus message). Lines 14 through 44 do not indicate the detail for each handshake cycle; they indicate only the transmission of the characters required for the programming commands and the subsequent transmission of the data by the DMM. Each transmission by the controller or the DMM, shown in lines 14 through 44, requires the handshake cycle illustrated by line entries 1 through 13 of the table.

Refer to table 4-8, line 1, and note that the first operation performed is the setting of the Remote Enable (REN) line to the low state. As explained in the table, this operation arms the bus members to go to the remote mode. The controller then transmits the interface clear (IFC) signal which stops bus activity and the attention (ATN) line is set low indicating that the next data byte placed on the bus by the controller will be a Bus Message. Note in the timing chart that when the ATN line is set low (3) that the DMM responds by setting the NRFD line high (4). This response by the DMM indicates that it is now ready to accept data.

When the DMM transmits the ready for data signal by setting the NRFD line high (line 4 of table 4-8) the controller puts the bus message UNL on the data lines. As shown in line 5 of the table this is the ASCII character ?. The unlisten message is a universal message understood by all bus members as the command "unlisten". Having placed the data character on the lines, the controller now says the data is valid by setting the DAV line low (6). The DMM then says: "I'm going to accept the data now on the data lines; don't change the data lines." The DMM then reads the data lines (8) and acknowledges acceptance of the data by setting the NDAC line high (9). The controller then removes the data valid signal (10), removes or changes data (11) and the DMM removes the data accepted signal from the bus (12).

At this point, one ASCII character has been transmitted by the controller to the DMM and the DMM is now ready to accept a new data byte. It indicates this (13) by setting the NRFD line high. The controller now puts the next character on the data line and the handshake cycle for the transfer of the character is repeated. The next character transmitted by the controller is the ASCII character U which is

the talk address of the Hewlett-Packard 9825 calculator. As indicated in table 4-8, by transmitting this character the calculator is making itself a talker. The next character transmitted is the quotation mark which is the listen address of the DMM when it has been assigned the decimal address 02.

Lines 16 through 24 of the table illustrate the sequence of transmission of the program string which instructs the DMM to make the DC voltage measurement. Lines 26 and 29 of the table indicate the end of transmission with the characters CR (carriage return) and LF (line feed). Note that at line 16 of the table the controller sets the ATN line high indicating that the program string to follow in lines 17 through 24 are device dependent messages.

Having transmitted the program string of device dependent messages to the DMM, the controller then sets the ATN line low which indicates that the characters to follow in lines 26 through 28 are bus messages. These bus messages change the talker/listener relationship of the controller and DMM; the DMM is made a talker and the controller becomes a listener.

Lines 30 through 44 illustrate the sequence of the transmission of data by the DMM. The handshake sequence is the same when the DMM is transmitting data as that outlined in lines 1 through 13 of the table, except that the DMM is controlling the handshake lines.

Upon completion of the data transmission, the DMM transmits a carriage return (CR) and line feed (LF) to indicate the end of the data transmission. Refer to table 4-9 for the GPIB programming requirements.

4-25. Interface Message Repertoire. The DMM is equipped with a standard GPIB interface which conforms to the specifications contained in IEEE-488-1978. The specification includes the definition of multi-line interface messages and this definition divides the messages into two groups: the primary command group and the secondary command group. The DMM includes none of the secondary command group in its interface message repertoire.

The primary command group of interface messages is further broken down into four lower categories: (1) the listen address group, (2) the talk address group, (3) the universal command group and (4) the addressed command group. The DMM is designed to include in its interface message repertoire 31 listen addresses and 31 talk addresses. The listen and talk addresses to which the DMM may be set are listed in table 4-7.

The interface messages to which the DMM is designed to respond are listed in table 4-10 with their decimal equivalents, hex equivalents, meanings, and data line codes. The function of the DMM in response to each of these commands is described in the following paragraphs.

4-26. Go To Local (GTL). As shown in table 4-10, the GTL command means go to local and the decimal and hex equivalent are both 01. Upon receipt of this interface message, the DMM, if previously programmed for remote, will return to its local operational state. This means that the instrument will then perform the function according to the settings of the front panel controls on the instrument until such time as it returns to remote control.

Table 4-9. GPIB Programming Requirements

1. Character Code: 7 bit ASCII, upper or lower case.

2. All program strings transmitted to the DMM should end in a terminating character. Acceptable terminators are:

   A. CR - Carriage Return

   B. LF - Line Feed

   C. EOI - This GPIB message EOI, true during transfer of the last byte of a string.

   D. X - ASCII letter.

3. Programming numerical constant over the GPIB
   The following units are assumed when programming numerical constants over the GPIB:

   Volts
   Kohms

Table 4-10. Interface Messages Used with Model 5005 DMM

Message	Meaning	HEX CODE	Decimal Equiv.	DATA LINE CODE						
				7	6	5	4	3	2	1
GTL*	Go To Local	01	1	0	0	0	0	0	0	1
SDC *	Selected Device Clear	04	4	0	0	0	0	1	0	0
GET *	Group Execute Trigger	08	8	0	0	0	1	0	0	0
LLO	Local Lock Out	11	17	0	0	1	0	0	0	1
DCL	Device Clear	14	20	0	0	1	0	1	0	0
SPE	Serial Poll Enable	18	24	0	0	1	1	0	0	0
SPD	Serial Poll Disable	19	25	0	0	1	1	0	0	1
UNL	Unlisten	3F	63	0	1	1	1	1	1	1
UNT	Untalk	5F	95	1	0	1	1	1	1	1

*Instrument will ignore message unless it is a listener

4-27. Selected Device Clear (SDC). Upon receipt of the SDC command, the DMM will go to the home state. The decimal and hex equivalent are both 04. The SDC message has the same effect as transmitting the GPIB program code 'Z' to the DMM.

4-28. Group Execute Trigger (GET). As shown in table 4-10, the decimal and hex equivalents of the GET command are both 08. Upon receipt of the GET interface message, the DMM will trigger a reading if it had previously been placed in the HOLD mode. The group execute trigger command is used to trigger the simultaneous execution of a number of functions by a number of bus members at the same time. To use this command, one or more bus members are programmed to perform a function on receiving the GET interface message. Subsequently, the controller will transmit the GET command and all bus members previously programmed will begin execution on receipt of the command.

4-29. Local Lock Out (LLO). The DMM may be brought back into local control by pressing the "Local" key on the keyboard. If, however, the DMM receives an LLO (Hex 11 or decimal 17) command while in remote operation, it may not be brought back into local control through keyboard operation.

4-30. Device Clear (DCL). The decimal equivalent of the DCL command (as shown in table 4-10) is 20, and the hex equivalent is 14. This command is identical in operation to the SDC command except that the DMM need not be a listener in order to respond to DCL. When this command is transmitted on the bus, all devices on the bus which respond to the DCL will clear. The DCL message has the same effect on the 5005 as transmitting the GPIB program code 'Z'.

4-31. Serial Poll Enable (SPE). As shown in table 4-10, the decimal equivalent of this interface command is 24; the hex equivalent is 18. The function of this command is to notify all bus members that they should output their serial poll status if made into a talker. Thus, when a bus member has transmitted a service request (SRQ), the bus controller can transmit the serial poll enable command, command each bus member to transmit its status byte by sequentially making each bus member a talker and thus identify the bus member requesting attention. Upon receipt of the DMM's talk address plus the SPE interface message, the DMM immediately prepares a status byte for transmission to the controller. If the DMM has previously transmitted an SRQ, it will set bit 7 of the status byte to 1. The serial poll allows a bus member to set the service request line to the 1 state, thus indicating to the controller that it wants attention. The controller may then sequentially interrogate each bus member to determine which one has requested service and the purpose of the request. The meanings of the bits in the status bytes are shown in figure 4-16.

4-32. Serial Poll Disable (SPD). As shown in table 4-10, the decimal equivalent to the SPD command is 25; the hex equivalent is 19. The function of this command is to return the bus members to their original states after the serial poll transaction has been completed.

4-33. Unlisten (UNL). As shown in table 4-10 the decimal equivalent of this command is 63; the hex equivalent is 3F. This command is also a universal interface message understood by all members of the bus as a command to go to the unlisten state. When this command is transmitted, all bus members previously in the listen state will return to the unlisten state.

STANDARD OUTPUT: ±D.DDDDD E ± DD CR LF

USED FOR OUTPUT OF READINGS AND
NUMERICAL CONSTANTS.

WHERE D = DATA BYTE
E ± DD = EXPONENT DATA BYTES
CR = CARRIAGE RETURN
LF = LINE FEED

OUTPUT UNITS (IMPLIED)

READING OUTPUT: VOLTS, OHMS

SERIAL POLL OUTPUT (SINGLE BYTE)

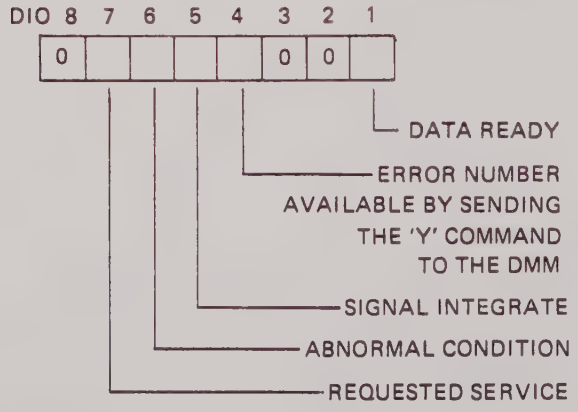

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Figure 4-16. GPIB Output Formats

4-34. Device Dependent Messages. The messages which control the operation of the DMM when in system operation are referred to as device dependent messages. These messages, listed in table 4-11, are simply combinations of ASCII characters which the instrument recognizes as specific instructions. To program the instrument for a specific operation, the operator programs the controller to transmit a sequence of these messages (referred to as a program string). The program string is variable in length and has no fixed format. Individual commands may be transmitted in any order and require no delimiters or spacing for the instrument to understand. A terminator character(s) should be sent as the last character in each program string. Acceptable terminators are CR (Carriage Return), LF (Line Feed), the GPIB message EOI in conjunction with the last byte of the string, also ASCII x lower case or X uppercase, or any combination of these. Most controllers will add terminator(s) to the program string automatically. Alphabetic characters may be either upper or lower case.

The device dependent messages are listed in table 4-11 with any special notes that apply. The device dependent messages applicable to the DMM are divided into subcategories such as Function Commands and Range Commands. In general, the various commands cause the instrument to perform the same functions as the front panel controls. There are special cases however, where there are extra functions available under remote control which are not available in the bench operation mode. Further, there are some special situations requiring special attention to the operation sequence used with the DMM.

To assemble a program string, first list the requirements of the program, and then select the appropriate program codes from table 4-11. Table 4-8 shows a program string listing for a typical measurement procedure.

4-35. Function Commands. Function commands are available to program the instrument to perform any Operation which may be commanded through use of front panel keyboard controls. Note that in table 4-11 the DMM operation column lists the functions available on the instrument and that the Program Code column shows the ASCII characters required to program the instrument for each of these functions. To program a function the controller need only transmit the ASCII characters required for the desired function (e.g., to program the measurement function DC volts, the controller simply transmits the two ASCII characters F and 1 over the bus to the DMM).

4-36. Range Commands. Seven individual range commands are available to the controller; one to command AUTO range and six additional commands for selecting specific ranges for the instrument. Note that the commands R3 through R7 all serve dual purposes; they command ranges for voltage measurements and for resistance measurements.

4-37. Trigger. Trigger commands T0 through T5 control the beginning of a measurement cycle. When the T1 command is transmitted, the instrument operates on the internal trigger on its normal measurement timing cycle (see figure 4-17). When the T2 command is transmitted, the instrument must be triggered by an external signal inputted through a BNC connector on the rear panel of the instrument. When the T3 command is transmitted, the instrument is put in the "Hold" state and will stay there until it is triggered either from the front panel or from the GPIB. Trigger commands from the GPIB can be either a T0 command or a Group Execute Trigger. Trigger commands are given from the keyboard by pressing 'Track' or 'Single' when the DMM is in local control. Upon receipt of the T4

Table 4-11. Model 5005 Device Dependent Program Code

INITIALIZE COMMANDS

Operation	Program Code	Special Notes
Initialize	Z	Same as G0T1N0

FUNCTION COMMANDS

Operation	Program Code	Special Notes
DC Volts	F1	
AC Volts	F2	
Ohms	F3	
Ohms	F4	

RANGE COMMANDS

Operation	Program Code	Special Notes
AUTO Range	R0	
.1V, .1KΩ	R3	
1V, 1KΩ	R4	
10V, 10KΩ	R5	
100V, 100KΩ	R6	
1000V, 1000KΩ	R7	
10000KΩ	R8	

TRIGGER COMMANDS

Operation	Program Code	Special Notes
Trigger Immediate	T0	Normally used in conjunction with T3.
Internal Trigger	T1	Causes continuous readings.
External Trigger	T2	Waits for trigger from rear panel BNC.
Hold/Manual	T3	Waits for trigger from GPIB or from keyboard.
External Trigger with Timeouts	T4	Same as T2 and T3 except than an internal time delay is inserted to allow for analog settling times.
Hold/Manual with Timeouts	T5	

Table 4-11. Model 5005 Device Dependent Program Code (Continued)

LOW/HIGH RESOLUTION COMMANDS

Operation	Program Code	Special Notes
4 1/2 digit display	I1	
5 1/2 digit display	I2	
	I3	

NULL COMMANDS

Operation	Program Code	Special Notes
Disable Null	N0	
Enable Null	N1	Subtracts null constant from reading.
Store as Null	N2	Stores previous reading or entered constant as null constant.
Transmit Null	N3	Output null constant to GPIB.

INTERRUPT COMMANDS

Operation	Program Code	Special Notes
No SRQ when Reading is Ready	D0	
SRQ when Reading is Ready	D1	
SRQ if Reading* is < 0	D2	
SRQ if Reading* is ≥ 0	D3	

*Reading after being modified by Null.

FILTER COMMANDS

Operation	Program Code	Special Notes
Filter Out	J0	
Filter In	J1	Selects the 3-pole active filter.

Table 4-11. Model 5005 Device Dependent Program Code (Continued)

EXTERNAL REFERENCE FUNCTION COMMANDS (SOFTWARE RATIO)

Operation	Program Code	Special Notes
Internal Reference	G0	Disables Software Ratio.
DC Reference	G1	Enable Software Ratio.
AC Reference	G2	
Ohms Reference	G3	
Ohms Reference	G4	

EXTERNAL REFERENCE RANGE COMMANDS

Operation	Program Code	Special Notes
AUTO Range	Q0	Returning the DMM to internal reference will not affect the external reference range setting.
.1V, .1KΩ	Q3	
1V, 1KΩ	Q4	
10V, 10KΩ	Q5	
100V, 100KΩ	Q6	
1000V, 1000KΩ	Q7	
10000KΩ	Q8	

ZERO COMMAND

Operation	Program Code	Special Notes
Ignored	K0	
Ignored	K1	
Zero Command	K2	DC Function 0.1V range (F1R3), must have been previously selected, and a short must be supplied across the input terminals.

COMMAND STRING TERMINATOR (OPTIONAL)

Operation	Program Code	Special Notes
Terminator	X	Use is required only when the DMM is being programmed from a controller which does not terminate the program string with a CR, LF or EOI.

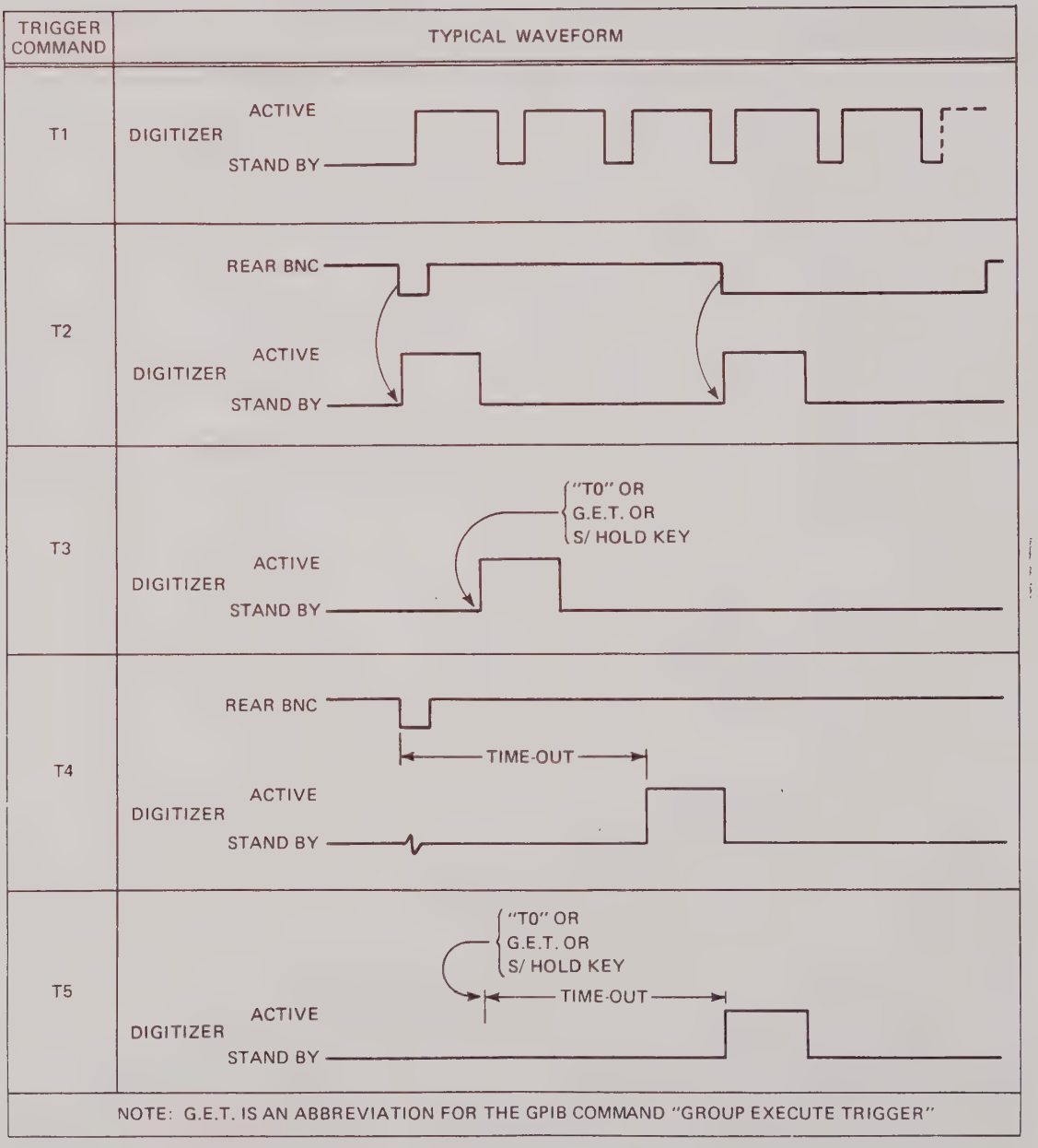
Table 4-11. Model 5005 Device Dependent Program Code (Continued)

ERROR OUTPUT COMMAND

Operation	Program Code	Special Notes
Error Output	Y	Output most recent error number.

CALIBRATION COMMANDS

Operation	Program Code	Special Notes
Decrease offset, this Range	K3	These commands have no effect unless the front panel calibration button is depressed.
Nominal offset, this Range	K4	
Increase offset, this Range	K5	
Decrease scale, this Range	K6	
Nominal scale, this Range	K7	
Increase scale, this Range	K8	



AUS036

Figure 4-17. Trigger Command Measurement Timing

program code the instrument goes into the External trigger mode and must be triggered by an external signal connected to the rear panel BNC connector. After being triggered via the rear panel BNC, the DMM executes a timeout which allows time for analog signals to settle. The timeout will vary, depending upon which functions and ranges are selected, before triggering a single reading. When program code T5 is transmitted, the instrument goes into the "Hold" mode described above except that its measurement cycle is again affected by the timeouts applicable to each function and range. For a complete description of 'TIME-OUTS' see paragraph 4-17.

4-38. HI-LO Resolution Commands. The measurement accuracy of the DMM is directly proportional to the signal integration time (i.e., the longer the integration time, the more accurate the measurement). If the measurement time is available, more accuracy may be obtained by programming the longer integration period. In situations where speed is required, the shorter integration time may be programmed at some sacrifice in measurement accuracy. The program codes I1, I2, and I3 select the resolution, the accuracy and the reading rate. Code I1 enables the 4 1/2 digit display which generates higher speed at the sacrifice of accuracy. Codes I2 and I3 develop greater accuracy at reduced speed.

4-39. Null Commands. Program codes N0 through N3 call for the Null functions. The N1 program code enables the Null function. Upon receipt of N1 from the interface, a flag is set in memory which signals the Computer to subtract the Null constant from future readings. The N2 program code allows for the storage of Null constants. Upon receipt of the N2 command, the previous reading or a constant entered via the GPIB is stored into memory for use as the Null constant. The N3 program code causes the DMM to transmit the Null constant to the controller.

The N1N2 program string accomplishes the same operation as selection of the "Null" key on the keyboard. Program code N0 disables the Null function but does not change the Null constant.

4-40. Interrupt Commands. Commands may be transmitted by the controller to instruct the DMM to transmit SRQ signals on the GPIB. When the controller transmits the D1 code, the DMM indicates the completion of each reading by sending a SRQ. If the D0 code is received, no SRQ will be sent upon completion of a reading.

4-41. Filter Commands. Control of the active filter in the remote mode is the same as manual control of the filter except that the controller transmits the program code commands J0 and J1 (as shown in table 4-11).

4-42. External Reference Function Commands. External reference function commands are used to select the voltage reference used by the digital multimeter in making measurements. The controller may select the normal internal reference or an external ratio reference. Transmission of the G0 program code by the controller causes the DMM to use internal reference for all measurements. When using the instrument in the external reference mode, the input signal is applied to the front panel or rear panel input terminals. The reference is applied to the front panel or rear panel reference terminals.

When using a DC external reference, the user first connects the signal and reference as described above and then transmits the program code G1. For AC

external reference, the same hook up is made followed by a G2 command. For ohms external reference, either the G3 or G4 command may be used.

4-43. External Reference Range Commands. There are six ranges for external reference signals applied to the external reference connector on the rear panel of the DMM. These are listed in table 4-11 under the Operation column heading. When using an external reference in remote mode, the controller must transmit the appropriate program code Q3 through Q8 to select the correct range. Q0 selects the reference AUTO range function.

4-44. Zero Commands. The code F1R3 must precede the Zero command code K2 to enable the Zero command. Furthermore, the HI-LO INPUT terminals on the front or rear panel of the DMM must be shorted.

4-45. Command String Terminator. The terminator code "X" permits the controller to terminate the program string when other terminating codes were not included in the string; typical terminators are CR, LF, or EOI. Most modern controllers will append a terminator to program strings automatically, making the use of 'X' program code unnecessary.

4-46. Error Output Command. When a programming error or operational error is discovered by the DMM when in remote, an SRQ is sent to the controller. Upon receiving the SRQ, the controller should read the DMM's status byte to determine why the SRQ was sent. If the status byte contains '1' in the DIO-4 position (see figure 4-17) then an error has occurred and an error number can be transmitted to the controller. To obtain this error message number, the controller first sends the program code 'Y' (why) to the DMM and then reads the error message number from the DMM. Table 4-5 can then be used to determine the nature of the problem.

4-47. Calibration Commands. If a CAL LAB is handling more than ten 5005 series voltmeters, it may be advantageous to automate the LAB calibration of the DMMs. To do this, the front panel "CAL" switch will be shorted on the main PCB and then commands K3 through K8 are transmitted to the DMM to modify its internal CAL constant. When the calibration is completed, the short across the CAL switch "must" be removed. Refer to paragraph 5-10 for additional details.

4-48. Initialize Command. The program code 'Z' is normally used by the controller to place the DMM into a known state. This program code is equivalent to the following string: G0T1N0.

G0 - Internal reference
T1 - Internal trigger
N0 - Disable NULL

4-49. Constant Manipulation from the GPIB. Two main buffers are used in GPIB operation (figure 4-18). The output buffer holds the ASCII characters which are waiting to be transmitted to the controller The input buffer has two uses. During the entry of numerical constants from the bus, the input buffer is used as the holding register. Also, the input buffer is used to hold the number which was most recently transferred to the output buffer. For instance, if given the command N2, the input buffer will contain the value of the null constant. Also, the output buffer will contain the ASCII characters corresponding to the null constant. If a reading is taken, it will be placed in both the input and output buffers.

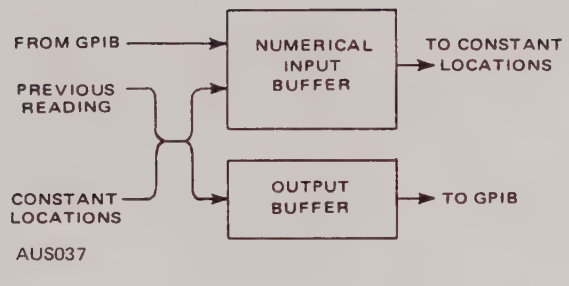


Figure 4-18. GPIB Input and Output Buffers

Whenever a 'store' command is executed, the present contents of the input buffer are stored in the given location. For instance, if a reading is completed and then a N2 command is given, the reading will be stored in as the NULL constant. If the command -2.05E-7N2 is executed, -2.05E-7 will be stored as the NULL constant.

4-50. TIME-OUTS: A PRACTICAL TREATISE. TIME-OUTS are variable delays which are inserted at the proper point in the measurement sequence in order to guarantee that the signal has settled sufficiently before a reading is taken.

The Model 5005 DMM provides 2 types of time-outs. Together these time-outs reduce the burden on the GPIB programmer because most of the system timing problems involving insufficient settling times and first reading errors are taken care of automatically inside the Model 5005. "First Reading Error" is an erroneous reading output by an instrument immediately following a function or range change.

Table 4-12 lists the time-out times and also lists the remaining digits of error which are not compensated for by the time-outs.

When the DMM is being programmed and triggered over the GPIB, a typical chain of events may occur something like this:

a. Apply input signal to DMM.
b. Program DMM and trigger reading.
c. Take reading from DMM.

Figure 4-19 shows this sequence graphically and also shows how the Model 5005 automatic timeout feature prevents it from outputting bad data after a function, range change, or other GPIB command. Notice in the figure that the input signal is assumed to have already settled before the sequence begins.

Another chain of events which commonly occurs is listed below. This situation is found more often when many inputs of the same type are being measured:

a. Apply input signal to DMM.
b. Trigger DMM (without changing function or range).
c. Take reading from DMM.

Figure 4-20 shows this sequence and also shows how the use of programmed time-outs (T4 and T5 cmds) allow the programmer to pass the responsibility for DMM settling time over to the 5005. Here again it is assumed that the input signal has already settled before the 5005 is triggered, since it would be impossible for the 5005 to compensate for an unknown settling time caused by conditions external to the DMM.

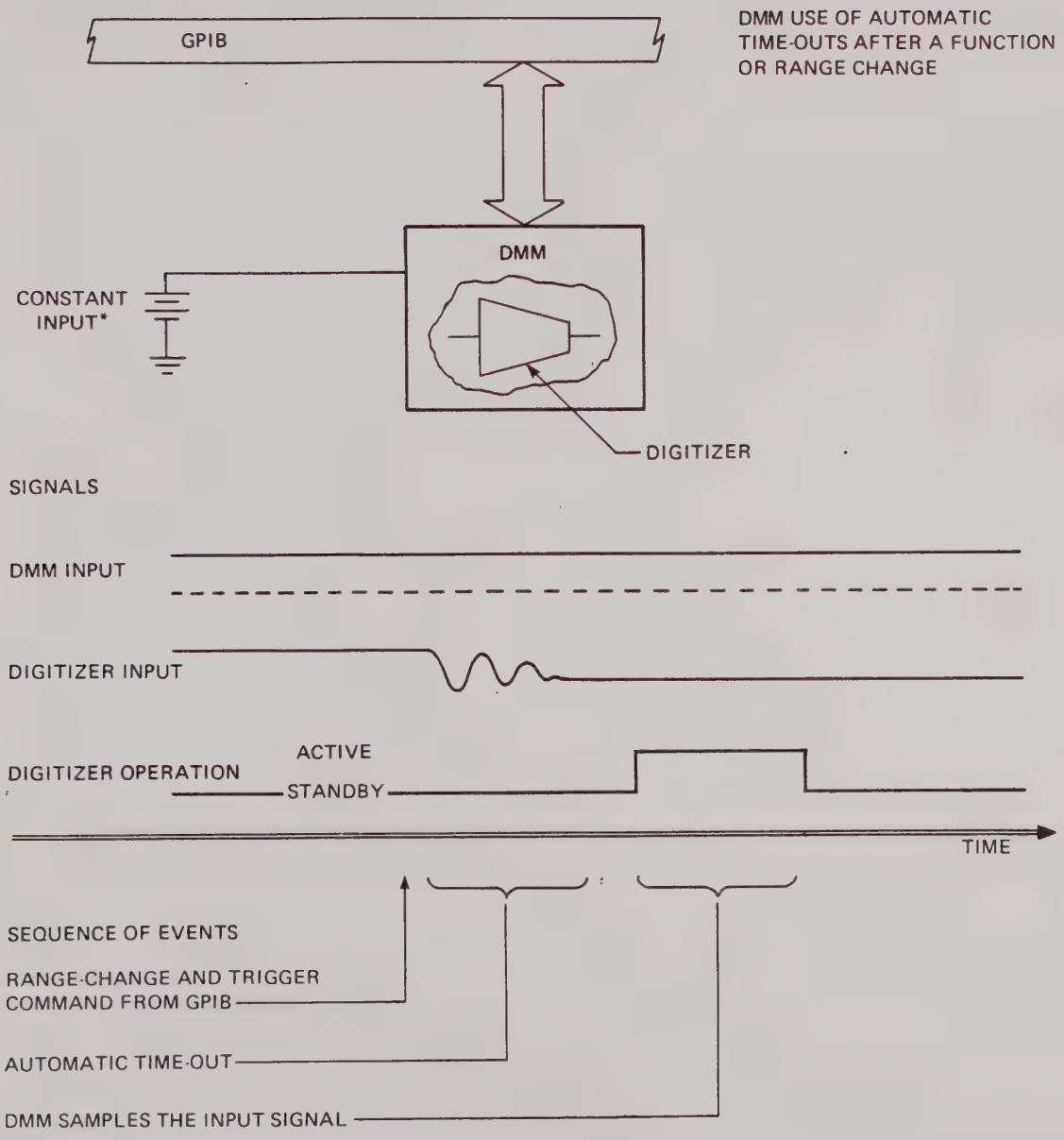
In the previous paragraphs it was mentioned how the 5005 handled its own settling time problems in various ways, but no mention was made of how the programmer might deal with settling time problems which originate external to the 5005. When low impedance measurements are being made, the main cause of delay times external to the DMM occur either in the signal source or in the signal scanner. Unless compensated for, these delays can cause large measurement errors.

One way of dealing with this situation is to place a delay in the controller's software between the signal setup routines and the DMM trigger routines, thus guaranteeing that the signal has settled before the DMM is triggered. A

Table 4-12. Time-Out Times

Function	Time-Outs	Digits Error	
		5 1/2 Mode	4 1/2 Mode
DC	30 mS	10	1
AC*	400 mS	100	10
K .1-1K	40 mS	10	1
10K	300 mS	10	1
Any Function Plus Filter	500 mS	10	1

*Time-out will be insufficient if incoming signal has a DC level other than zero volts.



*CONSTANT INPUT OR INPUT WHOSE SETTLING TIME IS VERY SMALL COMPARED TO THE APPLICABLE TIME-OUT TIMES

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Figure 4-19. DMM Automatic Time-Out

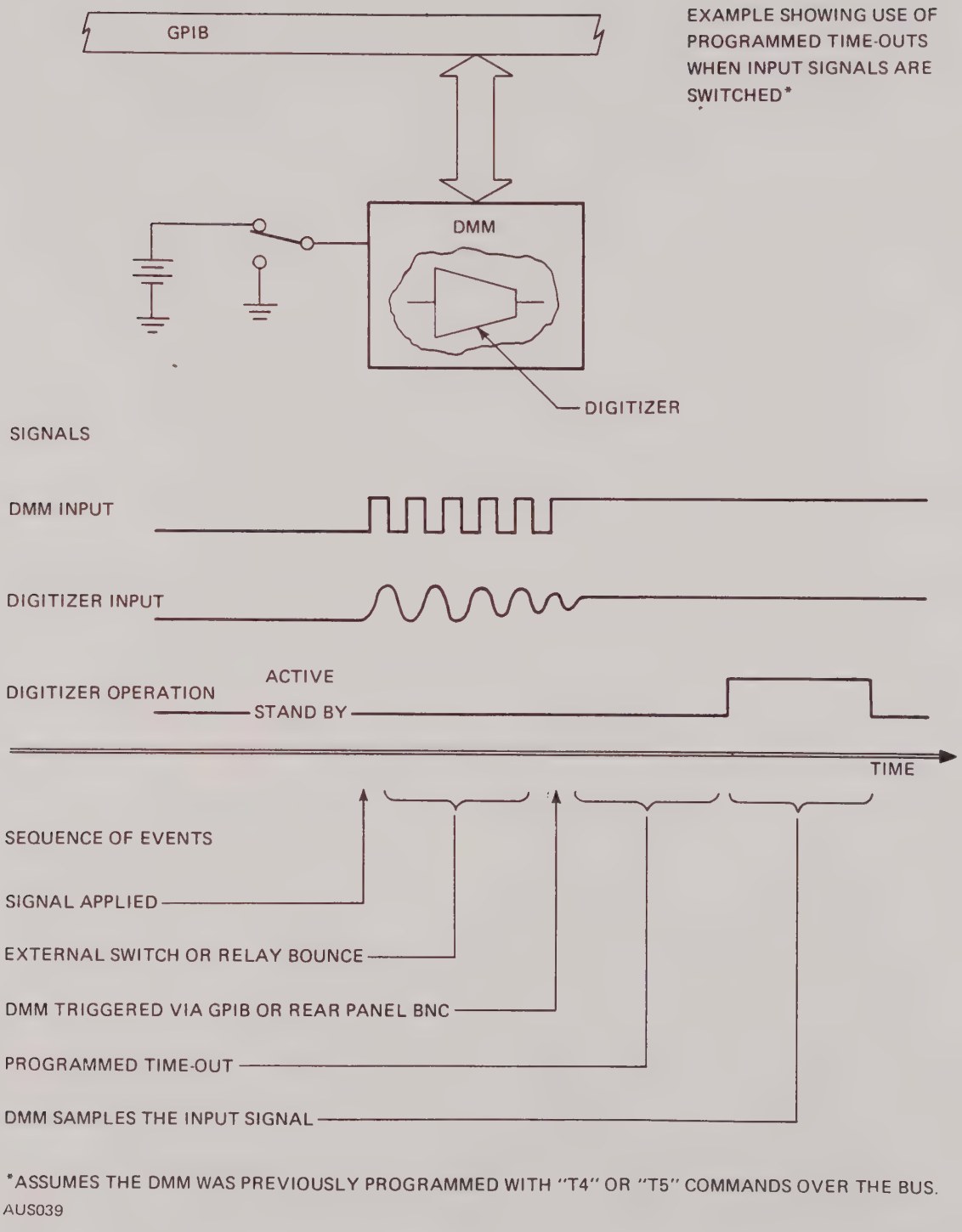

Figure 4-20. DMM Programmed Time-Out

complication arises because the required delay time may vary considerably depending upon which signal source function and range is selected, etc. In systems where test time is not critical, the programmer may decide to use the worst case required delay during all measurements.

If throughput is a consideration, the programmer may decide to use a variable delay which depends upon the selected signal source and scanner settings, but this approach may require intimate knowledge of the devices' internal workings or repeated experimentation.

4-51. GPIB THROUGHPUT CALCULATIONS: A PRACTICAL TREATISE. This description presents GPIB Throughput Calculations and is included as an aid to systems designers who must determine how much time is required to program, trigger, and obtain a reading from the Model 5005 DMM when operated over the GPIB.

The Handshake Times listed in table 4-13 are typical times required to handshake characters over the bus. These numbers can be used to estimate the bus time required to exchange various data. For an example, to transmit the string "F1R5CRLF" to the DMM (6 characters) 400 S/character = 2.4 mS are required approximately.

The time necessary to PROGRAM, TRIGGER and OUTPUT a reading from the DMM is presented in figures 4-21 and 4-22. Figure 4-21 is used when in the 5 1/2 digit mode or when in the 4 1/2 digit mode and the DMM is being programmed to the 5 1/2 digit mode. Figure 4-22 is used when the DMM is in the 4 1/2 digit mode or when the DMM is being programmed from 5 1/2 to 4 1/2 digit mode. Notice that the times shown do not include the actual bus time necessary to transfer data to or from the DMM, but this time can be estimated using table 4-13. The throughput equations shown in figures 4-21 and 4-22 are based upon the assumption that the DMM is in 'HOLD' and is waiting to be triggered or reprogrammed. This assumption is made because when not in hold, delays become much more difficult to estimate due to the random timing between incoming GPIB commands and readings already in progress. Since this text is an aid to computing the time required to obtain a reading, it is also assumed that each program string contains a DMM trigger such as the "TO" command, or is followed closely by a GET (Group Execute Trigger). This accounts for a Signal Integrate delay and also a reading being output to the GPIB.

Figures 4-21 and 4-22 show 2 GPIB lines at the top of the page. These are shown for reference only, and to identify when bytes are being transferred to or from the DMM. To ease the task of calculating DMM throughput, each figure is divided into three levels. Level 1 delays are the minimum delay that can occur whenever the DMM is programmed over the bus. GPIB commands which cause only Level 1 delays are those commands which cause no modifications to the instrument's hardware configuration. Examples of these are trigger commands, Null commands, R0 (autorange) command, and Z (initialize) command. These are all processed very rapidly, and the majority of Level 1 delays occur due to the "TO" or GET (Group Execute Trigger) which is assumed to accompany the program string.

If the GPIB command modifies one or more of the following: function, range, filter, front/rear control then Level 2 delays should be added to Level 1 delays when performing delay calculations. Examples of commands which will cause a Level 2 delay are: F1 (DC) if the DMM is in some other function, or R5 (10V range) if

Table 4-13. Typical GPIB Handshake Times

Bus Operation	Typical Time Req.
Handshake Interface Messages	12 Microseconds
Handshake and Process an Incoming String of Characters	400 Microseconds/Character
Output the Serial Poll Status Byte	300 Microseconds
Output a Reading (15 Characters)	130 Microseconds/Character

the DMM is in some other range. Note that Level 2 delays will only occur if the GPIB command modifies the function, range, etc. For instance, if the DMM is already in DC and the "F1" command is sent, only Level 1 delays will occur. Level 3 delays should be added if the DMM is being programmed from one digit mode (integrate time) to another. For example, if the DMM is in the 4 1/2 digit mode and an "I2" or "I3" command is received, the DMM will experience Level 3 as well as Level 1 and 2 delays.

4-52. INTERFACE ASSEMBLY OPERATION. The circuit breaker ON-OFF switch controls primary power to the Racal Dana DMM and the interface assembly. Pushbutton switch ZERO OHM is active when the DMM is under control of the AGERD and in Kohm and TRACK modes. When depressed, the resistance path is measured and the value subtracted from all subsequent ohms readings. This operation requires a short to be installed at the DMM input terminals. Some test programs require this short at the ITA to negate wiring and relay contact resistance.

The NORMAL-TRACK-REBAL switch is a three position switch. In NORMAL position, the DMM is under control of the AGERD. On station command, a reading will be initiated by the DMM. When the switch is positioned to TRACK, the Racal Dana DMM TRACK switch must be depressed to initiate tracking capabilities. The switch REBAL position is momentary and initiates a new reading. It can also be used to clear error conditions following an unsuccessful reading. Any such errors are indicated by the ERROR light or DMM BAL on DATAC. It will also provide a PRINT signal when the DMM is in the TRACK mode.

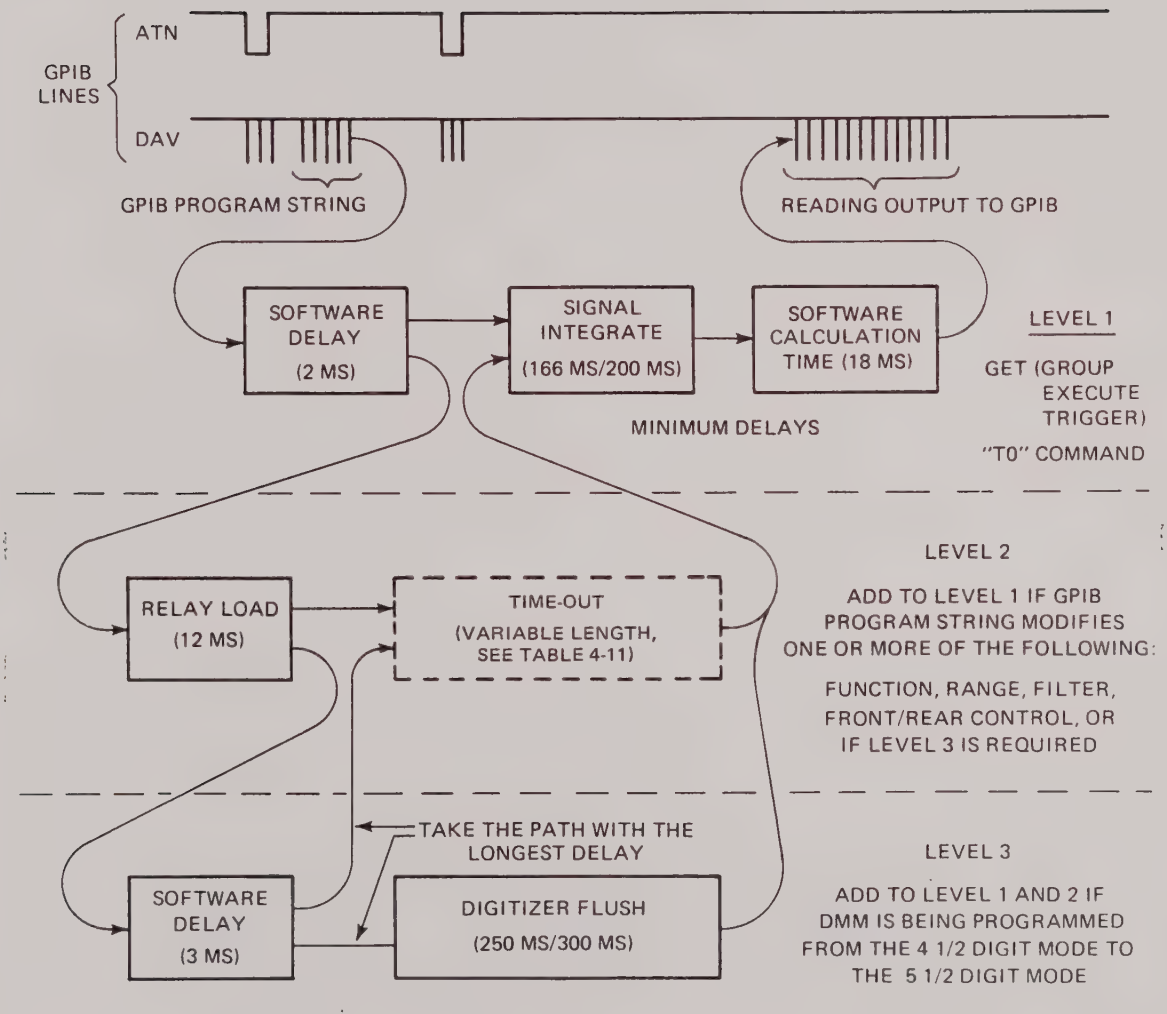
GPIB LINES
ATN
DAV
GPIB PROGRAM STRING
READING OUTPUT TO GPIB
SOFTWARE DELAY (2 MS)
SIGNAL INTEGRATE (166 MS/200 MS)
SOFTWARE CALCULATION TIME (18 MS)
MINIMUM DELAYS
LEVEL 1
GET (GROUP EXECUTE TRIGGER)
"T0" COMMAND
LEVEL 2
ADD TO LEVEL 1 IF GPIB PROGRAM STRING MODIFIES ONE OR MORE OF THE FOLLOWING:
FUNCTION, RANGE, FILTER, FRONT/REAR CONTROL, OR IF LEVEL 3 IS REQUIRED
RELAY LOAD (12 MS)
TIME-OUT (VARIABLE LENGTH, SEE TABLE 4-11)
TAKE THE PATH WITH THE LONGEST DELAY
SOFTWARE DELAY (3 MS)
DIGITIZER FLUSH (250 MS/300 MS)
LEVEL 3
ADD TO LEVEL 1 AND 2 IF DMM IS BEING PROGRAMMED FROM THE 4 1/2 DIGIT MODE TO THE 5 1/2 DIGIT MODE
TIME LEGEND: (60 Hz MACHINE/50 Hz MACHINE)
AUS040A

Figure 4-21. 5 1/2 Digit Mode Throughput Calculation

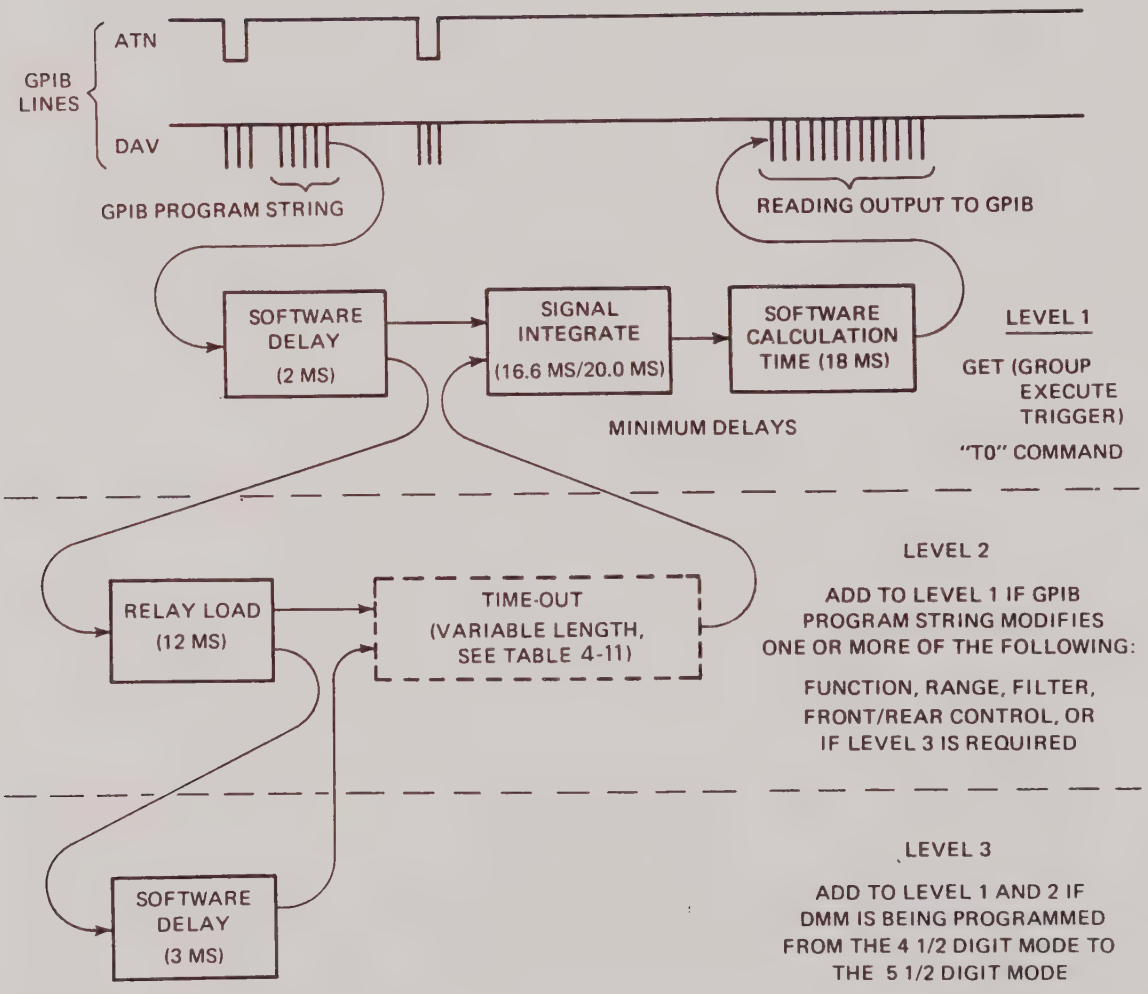
GPIB LINES
ATN
DAV
GPIB PROGRAM STRING
READING OUTPUT TO GPIB
SOFTWARE DELAY (2 MS)
SIGNAL INTEGRATE (16.6 MS/20.0 MS)
SOFTWARE CALCULATION TIME (18 MS)
LEVEL 1
GET (GROUP EXECUTE TRIGGER)
"T0" COMMAND
MINIMUM DELAYS
LEVEL 2
ADD TO LEVEL 1 IF GPIB PROGRAM STRING MODIFIES ONE OR MORE OF THE FOLLOWING:
FUNCTION, RANGE, FILTER, FRONT/REAR CONTROL, OR IF LEVEL 3 IS REQUIRED
RELAY LOAD (12 MS)
TIME-OUT (VARIABLE LENGTH, SEE TABLE 4-11)
LEVEL 3
ADD TO LEVEL 1 AND 2 IF DMM IS BEING PROGRAMMED FROM THE 4 1/2 DIGIT MODE TO THE 5 1/2 DIGIT MODE
SOFTWARE DELAY (3 MS)
TIME LEGEND: (60 Hz MACHINE/50 Hz MACHINE)
AUS041

Figure 4-22. 4 1/2 Digit Mode Throughput Calculation

SECTION 5

MAINTENANCE

5-1. RACAL DANA DMM MAINTENANCE.

5-2. Scope. Maintenance includes calibration checks and adjustment procedures required for routine service. Voltage measurements with waveforms tabulated under performance tests are supplied for troubleshooting guidance. A suggested equipment list is covered in table 5-1. In addition, the 9 program error message list is included with general troubleshooting information.

5-3. Calibration Check and Adjustment Procedures. This text contains procedures that compare the operation of the instrument against the specifications presented at the front of this manual. It is intended to be used as a periodic check to determine if the calibration of the instrument meets required specifications.

The procedures provide sufficient checks to verify proper operation and that the instrument is within the 6-month accuracy limits. The required ambient temperature of the environment is 23 ± 1 degree centigrade.

Remove the rear top cover item 3 page 6-41, figure 6-8, view A-A. Disconnect the banana plugs P1 through P5 (inputs and guard). Disconnect the Digital Multimeter power input plug. Connect ac power cable P/N 600620 or equivalent to digital multimeter power input receptacle and an external 115 Vac, 60 Hz power source. After calibration is completed, reconnect the digital multimeter to the interface assembly J5 and reinstall the rear top cover.

5-4. Required Equipment. A list of equipment required for calibration is given in table 5-1. The specific types of equipment suggested for calibration are listed under the Suggested Equipment heading. This list provides a guide for selecting suitable equipment having characteristics equal to or better than the items listed.

5-5. DC Voltage Sources. To produce voltage levels of necessary accuracy, special techniques are required. Suitable methods of generating these voltages are shown in figures 5-1 and 5-2 and tables 5-2 and 5-3. A precise and traceable source of 10 volts is required, not only for calibrating the 10 volt range, but also as a reference for generating highly accurate .1, 1, 100, and 1000 volt levels. The 10 volt source used must satisfy the following requirements:

a. It must be traceable to the National Bureau of Standards;
b. It must have a total accuracy of 2 ppm;
c. It must have a low output impedance.

A source filling these requirements is shown in figure 5-1. This circuit consists of a null detector, 7-decade voltage divider, a DC voltage supply, and a bank of saturated standard cells. Two advantages of this particular hookup are that: (a) there is minimal loading of the standard cells and (b) stability, not accuracy, is

the primary requirement of the DC voltage supply. The output of this circuit is set to a precise 10 volts by setting the voltage divider to the value of the standard cells. The DC voltage source is then adjusted to produce a null on the null detector. The accuracy of the 10 volt source is within 2 ppm. The remainder of the DC sources can be generated by the circuits shown in tables 5-4 and 5-5. Each of these hookups use a calibrated 10 volt source having the characteristics of the one previously described.

Table 5-1. Required Equipment

Function	Qty	Item	Minimum Use Specifications	Suggested Equipment
DC	(1)	Saturated Standard Cell Bank (6 cells)	1 ppm, certified	EPPLEY 106
	(2)	DC Voltages Sources	0.1 ppm resolution	FLUKE 332B
	(2)	Voltage Dividers, Adjustable	< 1 ppm linearity	FLUKE 720A
	(1)	Decade Resistance Box		ESI DB62
	(2)	Null Detector/μ Voltmeters	1 μV sensitivity	FLUKE 845AR
AC	(1)	Thermal Transfer Standard	50 ppm	HOLT 6A, With corrections
	(1)	AC Voltage Source	1 ppm resolution	HP745A/746A
Ω	(8)	Resistance Standards	Known within:	
		100Ω	10 ppm	ESI SR1 with corrections
		1 KΩ	10 ppm	ESI SR1 with corrections
		10 KΩ	10 ppm	ESI SR1 with corrections
		100 KΩ	10 ppm	ESI SR1 with corrections
		1 MΩ	10 ppm	ESI SR1 with corrections
		10 MΩ	20 ppm	ESI SR1 with corrections
OTHER	(1)	Momentary Switch, SPST	–	–
	(2)	1.5 volt cells w/screwtype binding posts	–	–
	(1)	Insulated Adjustment tool	–	JFD5284
	(1)	100Ω, 10 Kilohm, 1 Megohm 1/4 Watt 5% Carbon Resistors	5%	–
	(1)	1 μFD non polar capacitor	–	–

Table 5-2. DC Source Accuracies

Range	10 Volt Source	Voltage Divider	Total Accuracy	24 hr. DMM Full Scale Accuracy	Times Better
10	2 ppm	–	2 ppm	80 ppm	40
1	2 ppm	1 ppm	3 ppm	80 ppm	27
100mV	2 ppm	1 ppm	3 ppm	90 ppm	30
100	2 ppm	1 ppm	3 ppm	80 ppm	27
1000	2 ppm	1 ppm	3 ppm	80 ppm	27

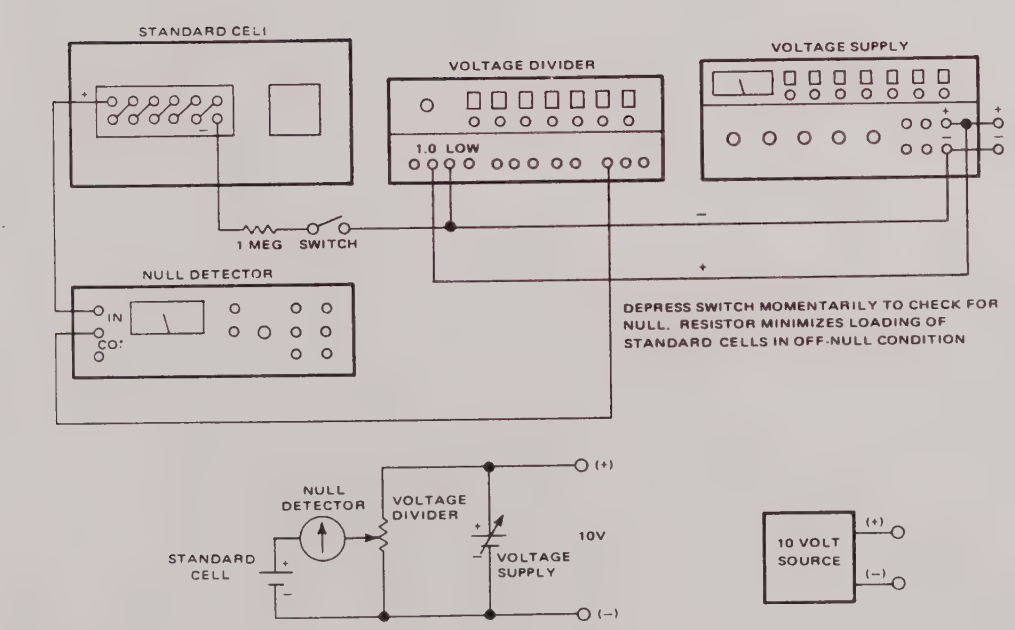

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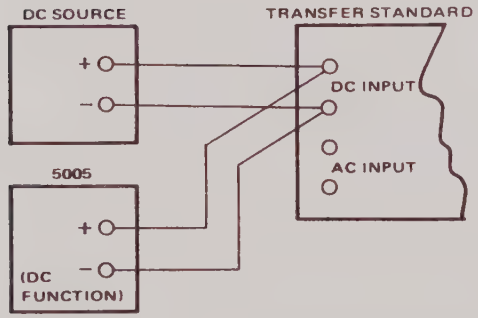
Figure 5-1. 10 Volt Source

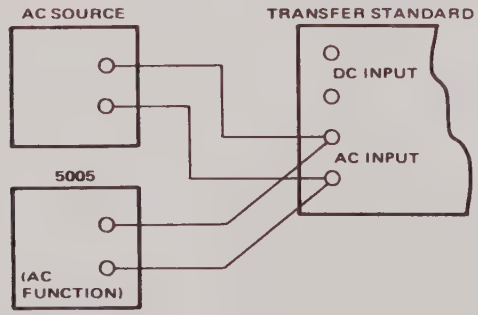
Table 5-3. AC Source Accuracies

INPUT		ACCURACY		
AC Source				
Volts	Freq	Thermal Transfer Standard	DC* Source	Total AC Source
1.0V	30 Hz	.005%	.012%	.017%
10V	to	.005%	.014%	.019%
100V	15 KHz	.01%	.014%	.024%
500V		.01%	.014%	.024%
1 KV		.02%	.014%	.034%

*6-month accuracy of 5005 DMM monitoring DC source on transfer standard.



DC. With DMM used to monitor DC output, DC source is adjusted to desired voltage. Transfer standard is then used per manufacturer instructions.



AC. The ac source is adjusted to produce a null on transfer standard. The AC source output is now calibrated and can be used as a precision source for the recalibration of the AC Converter.

NOTE: Because of the low input impedance of the transfer standard, the DMM input leads must be connected as close to the transfer standard input terminals as possible.

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Figure 5-2. AC Source

Table 5-4. DC Function Check (Low Ranges)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	DC VOLTAGE STANDARD	VOLTAGE DIVIDER SETTING			
DC	.1V	10.00000	.01000	.100000	.099985 – .100015	23°C ± 1°C (After Zero Command)
		10.00000	.02000	.200000	.199975 – .200025	
	1V	10.00000	.10000	1.00000	.99988 – 1.00012	
		10.00000	.20000	2.00000	1.99980 – 2.00020	

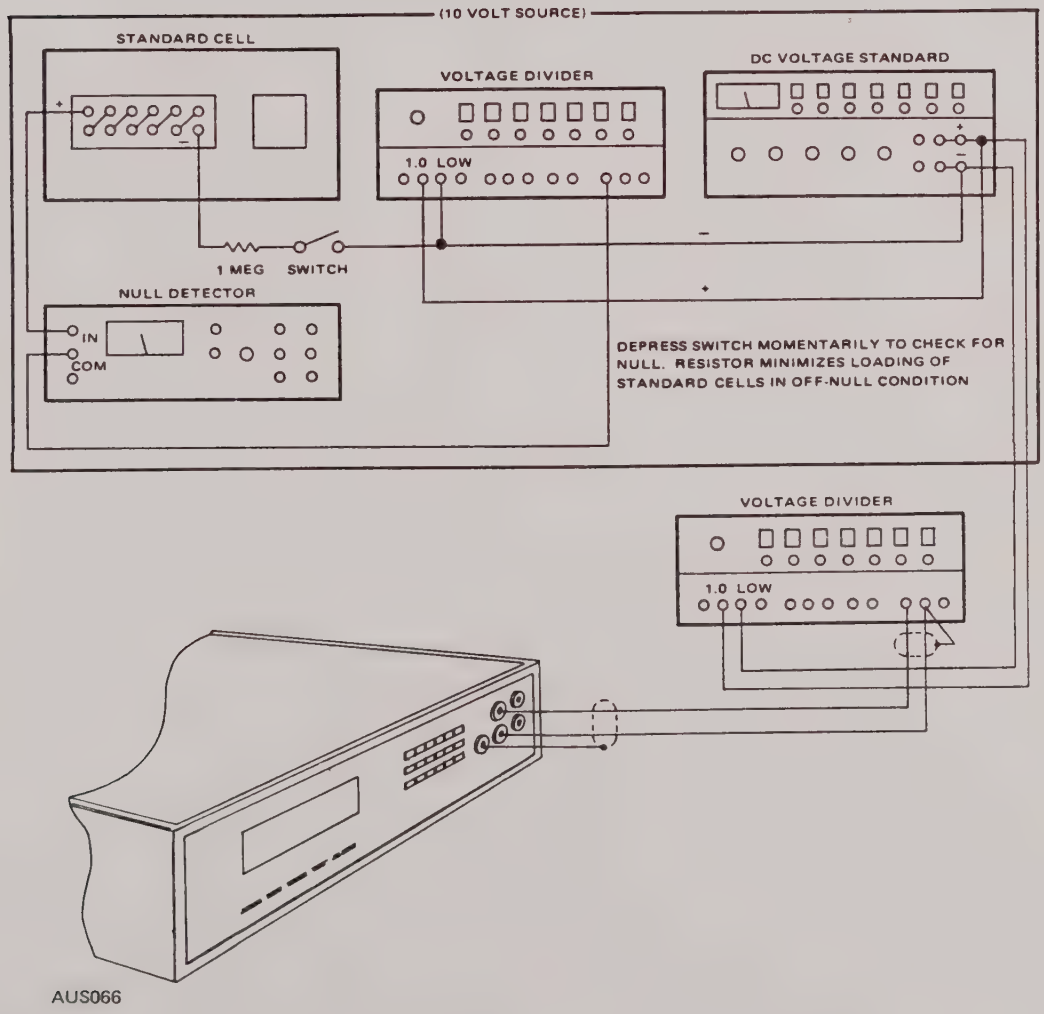

Figure 5-3. DC Function Check (Low Ranges)

Table 5-5. DC Function Check (High Ranges)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	DC VOLTAGE STANDARD	VOLTAGE DIVIDER SETTING			
DC	10	10.0000V	1.0000	10.0000	9.9986 – 10.0014	23°C ± 1°C (After Zero Command)
		20.0000V	.50000	20.0000	19.9976 – 20.0024	
	100	100.000V	.10000	100.000	99.986 – 100.014	
		200.000V	.05000	200.000	199.976 – 200.024	
	1000	1000.00V	.01000	1000.00	999.86 – 1000.14	

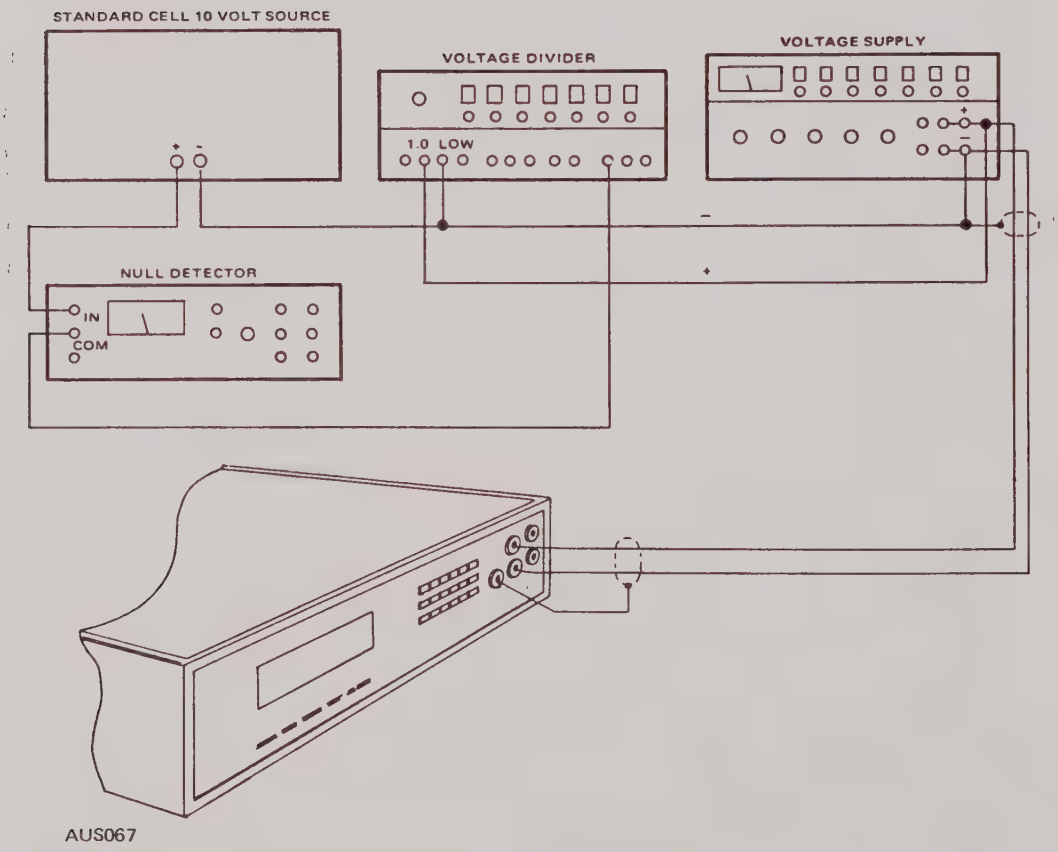

Figure 5-4. DC Function Check (High Range)

5-6. DC Accuracy. The accuracy of the DC voltage sources is obtained by adding the various sources of error in each hookup; errors in this discussion are defined in parts per million (ppm). For the 10 volt source, the error is the sum of the standard cell bank (certified at 1 ppm) and the voltage divider (1 ppm), giving a total error of 2 ppm. Table 5-2 shows the errors of each voltage source, the total accuracy of each hookup, the accuracy of the DMM, and the degree to which the sources exceed the required accuracy of the DMM (4 to 10 times better is the suggested accuracy ratio per MIL-M-38793).

5-7. AC Voltage Sources. The generation of accurate AC signals for checking the AC Converter ranges, requires the use of a thermal transfer standard and a precise DC standard as well as a stable AC source. Sufficient accuracy can be obtained by using a DC source and the DMM being tested. The circuitry connections are shown in figure 5-2. Information on the use of the transfer standard can be obtained from the operators manual accompanying the standard. The DMM is used to set the DC source to the desired voltage; the thermal transfer standard is then used to calibrate the output of the AC source. The calibrated AC source is used to check the AC converter. This procedure is repeated for each range.

5-8. AC Accuracy. The accuracy of the AC source is equal to the sum of the transfer standard accuracy and the accuracy of the DC source. The accuracy of the setup for each range and frequency used is provided in table 5-3.

5-9. Test Procedures. Allow two hours for warmup. Connect the instrument and the test equipment as shown in the figure supplied with each accuracy check. Select the controls and inputs as called out in the tables and monitor the instrument readout for the indicated values. Proceed with the tests described in tables 5-4 through 5-9.

WARNING

The following procedures include the use of high voltage sources producing potentially lethal voltages. Do not contact high voltage terminals.

5-10. The Model 5005 Calibration Principles. This calibration procedure for the 5005 DMM utilizes microprocessor controlled adjustments. The calibration adjustments executed through the keyboard input or GPIB commands are the software method of setting correction factors. The mechanical adjustments of three potentiometers are for DC, AC and Resistance zero offsets only.

The Non-Volatile Constants memory of the DMM enables the microprocessor to program software calibrations. Inputs are applied to the DMM from the calibration standard and the reading is incremented or decremented via keyboard control or GPIB commands until the reading equals the input standard. During this process, the numeric constants for analog offset voltages and scale factor corrections are loaded into the Non-Volatile memory by the microprocessor. These constants are then used by the microprocessor to correct DMM reading that appears on the display or to propagate to GPIB.

To enter correction constants into the Non-Volatile memory, three conditions are required:

a. The correct input standard for the function and range selected is applied to the DMM.

Table 5-6. Average AC Function

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	DC VOLTAGE STANDARD	RMS VALUE			
AC	1	1.000000	1V @ 30 Hz	1.00000	.99570 – 1.00430	23°C ± 1°C
		1.000000	1V @ 15 KHz	1.00000	.99880 – 1.00120	
	10	10.00000	10V @ 30 Hz	10.0000	9.9570 – 10.0430	
		10.00000	10V @ 15 KHz	10.0000	9.9880 – 10.0120	
	100	100.0000	100V @ 30 Hz	100.000	99.570 – 100.430	
		100.0000	100V @ 15 KHz	100.000	99.880 – 100.120	
	1K	1000.000	1000 V @ 30 Hz	1000.00	994.70 – 1005.30	
		1000.000	1000V @ 15 KHz	1000.00	997.80 – 1002.20	

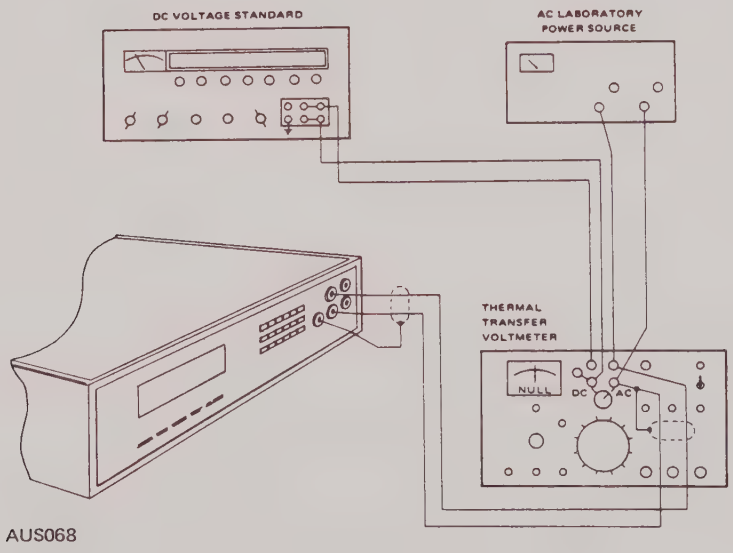

Figure 5-5. Average AC Function

Table 5-7. K Ohms Function

DVM		INPUT SIGNAL		NOMINAL READING (Same as Standard)	TOLERANCE* (6 MO. SPEC.) 5-1/2 DIGIT MODE
FUNCTION	RANGE	NOMINAL STANDARD VALUE	STANDARD VALUE KNOWN TO WITHIN:		
ʃ KΩ Ω	.1KΩ	100Ω	.001%		± 36 digits
	1 KΩ	1 KΩ	.001%		± 36 digits
	10 KΩ	10 KΩ	.001%		± 36 digits
	100 KΩ	100 KΩ	.001%		± 36 digits
	1000 KΩ	1 MΩ	.001%		± 36 digits
	10000 KΩ	10 MΩ	.001%		± 36 digits

*After Zero Command and Null Command.

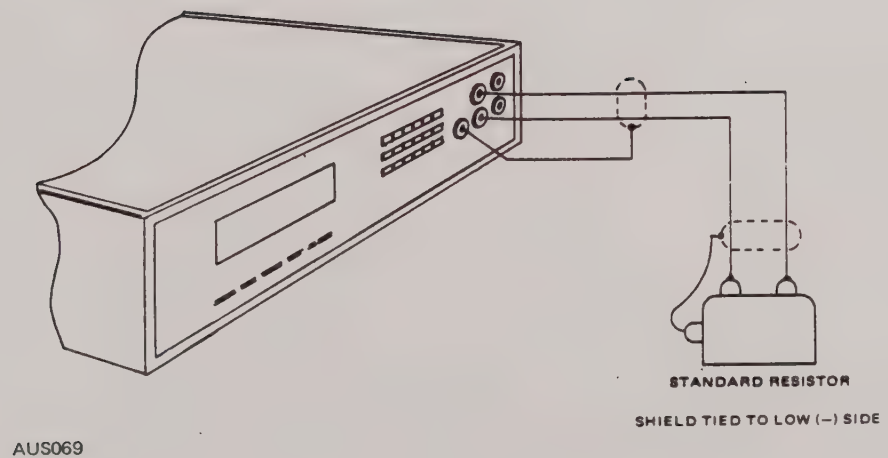

Figure 5-6. K Ohms Function

Table 5-8. Normal Mode Noise Rejection (In DC Volts Function)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE	NOTE
FUNCTION	RANGE	DC	AC			
DC FILT. OUT	10	0.5V	7.07V RMS 60 Hz*	00.5000	± 1000 digits	

*50 Hz for 50 Hz Instruments.

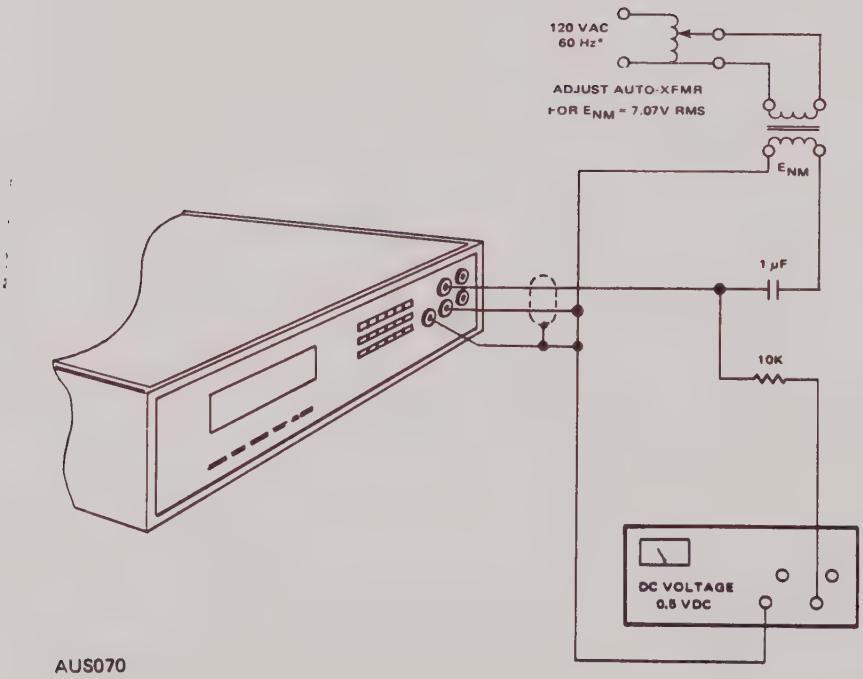

Figure 5-7. Normal Mode Noise Rejection (in DC Volts Function)

Table 5-9. Common Mode Rejection (In DC Volts Function)

DVM		INPUT SIGNAL		NOMINAL READING See Note 1	TOLERANCE	NOTE
FUNCTION	RANGE	S1				
DCV	1V	Off				1) With switch S-1 in the off position, record the reading displayed on the DMM's readout in the "nominal reading" boxes of the table.
		DC	1000V		± 10 digits from nominal	
		AC	107V RMS 60 Hz*		30 digits peak-to-peak	

*50 Hz for 50 Hz Instruments.

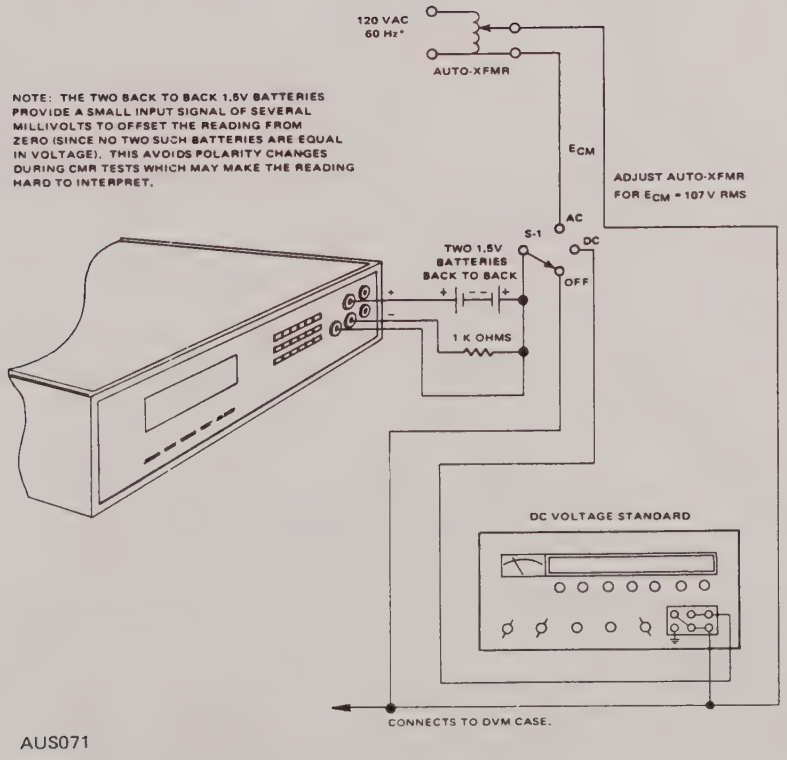
120 VAC
60 Hz*
AUTO-XFMR
NOTE: THE TWO BACK TO BACK 1.5V BATTERIES PROVIDE A SMALL INPUT SIGNAL OF SEVERAL MILLIVOLTS TO OFFSET THE READING FROM ZERO (SINCE NO TWO SUCH BATTERIES ARE EQUAL IN VOLTAGE). THIS AVOIDS POLARITY CHANGES DURING CMR TESTS WHICH MAY MAKE THE READING HARD TO INTERPRET.
E_{CM}
ADJUST AUTO-XFMR FOR E_{CM} = 107 V RMS
AC
S-1
DC
OFF
TWO 1.5V BATTERIES BACK TO BACK
1 K OHMS
DC VOLTAGE STANDARD
CONNECTS TO DVM CASE.
AUS071

Figure 5-8. Common Mode Rejection (in DC Volts Function)

b. The calibration switch (Cal-Sw) must remain depressed during the adjustment process.

c. A keyboard input or GPIB command is required to increment or decrement the reading to equal the input standard.

NOTE

Keyboard or GPIB calibration commands are "not" effective unless the CAL-SW is held in the depressed position. Numbers are entered into the non-volatile memory only when the Cal-Sw is in the "depressed position."

The Cal-Sw is a momentary contact switch accessible through an opening on the front panel (see figure 4-1 No. 8 for location). The switch can be depressed by inserting an appropriate size screwdriver or similar tool through the opening.

The DMM Function, Range and Input Standard for each entry into the Non-Volatile memory is listed in table 5-11. One offset correction factor is entered for each Function and a scale factor is entered for each Range. In the DC Function, scale factors are entered for both positive and negative inputs, additionally a scale factor correction constant is entered for the 4 1/2 digit mode. Refer to table 5-10 for details.

The DMM procedure to enter corrections are as follows:

a. Offset Correction Factors: Zero volts or ohms are applied to the DMM.

b. Scale Factor Corrections: A full scale input is applied in each Function and Range.

c. Three input keys on the keyboard which perform the UP count, DOWN count, and NOMINAL functions are described below.

(1) UP Key: Performed by depressing the SINGLE key the numbers in memory while the Cal-Sw is held depressed.

(2) DOWN Key: Performed by depressing the LOCAL key and referred to as LOCAL/DOWN. This key decrements the numbers in memory while the Cal-SW is held depressed.

(3) NOMINAL Key: Performed by depressing the RESET key and referred to as RESET/NOMINAL. This key initializes the numbers in memory while the Cal-Sw is held depressed, as explained in the next paragraph.

The RESET/NOMINAL key is used to initialize the numbers in Non-Volatile memory. When this key is depressed and released, either a ZERO is entered into the Non-Volatile memory as an offset correction factor, provided the DMM input is less than 40% of full scale, or a ONE is entered into the Non-Volatile memory as a scale factor, provided the DMM input is greater than 40% of full scale.

Table 5-10. Non-Volatile Memory Constants

Memory Constant	Calibration Conditions		
	Function	Range	Input
DC Offset	DC	.1V	Zero
.1V Pos. Scale Factor	DC	.1V	+.1VDC
.1V Neg. Scale Factor	DC	.1V	−.1VDC
1V Pos. Scale Factor	DC	1V	+1VDC
1V Neg. Scale Factor	DC	1V	−1VDC
10V Pos. Scale Factor	DC	10V	+10VDC
10V Neg. Scale Factor	DC	10V	−10VDC
100V Pos. Scale Factor	DC	100V	+100VDC
100V Neg. Scale Factor	DC	100V	−100VDC
1KV Pos. Scale Factor	DC	1KV	+1KVDC
1KV Neg. Scale Factor	DC	1KV	−1KVDC
4 1/2 Digit Scale Factor	DC	1V	± 1VDC
AC Offset	AC	1KV	Zero
1V Scale Factor	AC	1V	1V RMS, 400 Hz
10V Scale Factor	AC	10V	10V RMS, 400 Hz
100V Scale Factor	AC	100V	100V RMS, 400 Hz
1KV Scale Factor	AC	1KV	1000V RMS, 400 Hz
Ohms Offset	Ω	100K	Zero
.1K Scale Factor	Ω	.1K	100Ω
1K Scale Factor	Ω	1K	1KΩ
10K Scale Factor	Ω	10K	10KΩ
100K Scale Factor	Ω	100K	100KΩ
1000K Scale Factor	Ω	1000K	1MΩ
10,000K Scale Factor	Ω	10,000K	10MΩ

Table 5-11. Calibration Points for Entry of Final Values Into Non-Volatile Memory

Function	Range	Input Standard	Input Connections	Notes
DC	.1V	0.00000 VDC	Table 5.4	Note 1 - See paragraph 5.1.5.13 to calibrate 4 1/2 Digit mode.
	.1V	+0.1 VDC		
	.1V	−0.1 VDC		Note 2 - The value of the Resistance Standard must be known to within the tolerance indicated in Table 5.1.
	1V	+1.0 VDC		
	1V	−1.0 VDC		
	1V	(Note 1)		
	10V	+10.0 VDC	Table 5.5	Note 3 - Lead resistance will cause an error in the 100Ω and 1KΩ ranges. When performing final calibration to these ranges, note the error by shorting the test leads together at the ohms source and reading the display. The 100Ω and 1KΩ ranges should be cali-
	10V	−10.0 VDC		
	100V	+100.0 VDC		
	100V	−100.0 VDC		
	1KV	+1000.0 VDC		
	1KV	−1000.0 VDC		

Table 5-11. Calibration Points for Entry of Final Values Into Non-Volatile Memory (Continued)

Function	Range	Input Standard	Input Connections	Notes
AC	1KV 1V 10V 100V 1KV	0.0V RMS 1.0V RMS, 400 Hz 10.0V RMS, 400 Hz 100.0V RMS, 400 Hz 1000.0V RMS, 400 Hz	Table 5.6	brated high by the amounts of error noted in these two respective ranges. The NULL command will be used by the operator to remove the lead resistance error in his measurement application, but cannot be used during Lab Cal to remove the effects of lead resistance.
OHMS	100KΩ .1KΩ 1KΩ 10KΩ 100KΩ 1000KΩ 10,000KΩ	0.0Ω 100.0Ω (Note 2) 1.0KΩ (Note 3) 10.0KΩ 100.0KΩ 1.0MΩ 10.0MΩ	Table 5.7	

The LOCAL/DOWN key decrements the numbers in the Non-Volatile memory. This action is described as follows:

a. When entering an offset correction factor, this key changes the reading in a "Negative going" direction. For example, if the DMM reading is .00023 for zero input in the DC function, each time the LOCAL/DOWN key is depressed and released, the reading will decrease one digit. Upon reaching .00000, calibration of the DC offset correction factors is complete. Further depression of this key will cause the reading to increase with a negative polarity indication.

b. When entering scale factors, each depression of the LOCAL/DOWN key will decrease the displayed reading one digit when a Full Scale Input is applied.

c. When the decrements required for corrections are numerous, holding the LOCAL/DOWN key depressed longer than 2 seconds approximately, will decrement the readings as a faster rate as long as the key remains depressed.

The SINGLE/UP key increments the numbers in the Non-Volatile memory. This action is described as follows:

a. When entering an offset correction factor, this key changes the reading in a "Positive going" direction. For example, if the DMM reading is -.00023 for zero input in the DC Function, each time the SINGLE/UP key is depressed and released, the reading will decrease one digit. Upon reaching .00000, calibration of the DC offset correction factor is complete. Further depression of this key will cause the reading to increase with a positive polarity indication.

b. When entering scale factors, each depression of the SINGLE/UP key will increase the display reading one digit as a Full Scale input is applied.

c. When the increments required for corrections are numerous, holding the SINGLE/UP key depressed longer than 2 seconds approximately, will increment the readings at a faster rate as long as the key remains depressed.

When calibration is performed via the GPIB, it is convenient to short the Cal-Sw terminals with a temporary jumper. The Cal-Sw drawing shown in figure 5-9 indicates the location of the jumper.

WARNING

These servicing instructions are for use by qualified personnel only To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

CAUTION

Connect the jumper after power is applied to the DMM and disconnect the jumper before power is removed. If this instruction is not followed, the contents of the Non-Volatile memory will be destroyed and "Error 4" will be displayed the next time power is applied to the DMM.

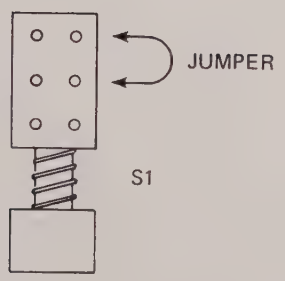

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Figure 5-9. Cal-Switch

GPIB commands K3 through K5 affect the Offset constant for the Function which is presently programmed. Each transmission of the K3 or K5 command to the DMM is equivalent to applying a low-level input (Low level is less than 40% and high-level is greater than 40% of Full Scale.), and momentarily pressing the LOCAL/DOWN or SINGLE/UP keys on the DMM front panel. Transmitting the K4 command is equivalent to the keyboard procedure for initializing offset constants, with the exception that the input signal need not be less than 40% of full scale when initializing offset constants over the bus.

GPIB commands K6 through K8 affect the Scale constants for the range which is presently programmed. Each transmission of the K6 or K8 command to the DMM is equivalent to applying a high level input and momentarily pressing the LOCAL/DOWN or SINGLE/UP keys on the DMM front panel.

Transmitting the K7 command has the same effect as initializing scale constants from the keyboard. To initialize a scale factor over the GPIB, the following procedure is provided:

a. Apply a high-level input signal.
b. Complete a least one reading on the presently programmed function/range.
c. Transmit the K7 command to the DMM.

NOTE

The K4 and K7 commands should not be required unless the contents of the non-volatile are destroyed.

In situations where the input standard and the initial reading differ by several hundred digits, the difference can be reduced at the fastest rate by switching to the 4 1/2 digit mode (depress and release RESOL key). In the 4 1/2 digit mode, each depression of the SINGLE/UP or LOCAL/DOWN key changes the reading one digit, which is 10 digits on the 5 1/2 digit mode. Holding either key depressed for fast increment or decrement operation also changes the reading in 10 digit increments. Once the reading has been reduced to within 10 or 20 digits of the input standard in the 4 1/2 digit mode, switch back into the 5 1/2 digit operation to complete the calibration.

When using the 4 1/2 digit mode to change the reading rapidly, the DMM "must be in a fixed range" (AUTO ranging disabled and AUTO annunciator off). If this precaution is not taken, the 4 1/2 digit Scale Factor will be modified instead of the desired Non-Volatile memory constant.

If the 4 1/2 digit Scale Factor is inadvertently modified, the 4 1/2 and 5 1/2 digit readings will differ. The following procedure can be used to reinitialize the 4 1/2 digit Scale Factor:

a. Select the DC Function any Range, 4 1/2 digit mode, Auto-ranging (Auto-annunciator ON).

b. Apply a full scale input to the DMM for the Range selected in (a.).

c. Depress and hold the calibration switch.

d. Depress and release the RESET/NOMINAL key.

e. Release the calibration switch.

5-11. Calibration Procedure.

5-12. Test Point Locator. The test points specified during calibration are noted on figure 5-10, a reproduction of the motherboard.

5-13. Ohms Amplifier Offset Zero (R1).

a. Short the INPUT terminals and GUARD terminal together.

b. Select DC Function, .1V Range.

c. Allow instrument at least one hour warm up with covers in place.

d. Hold the .1 Range key depressed, until "CAL 0" appears on the display, then release the key.

WARNING

These servicing instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

e. Remove top cover.

f. Select OHMS Function, 100KΩ Range.

g. Adjust R1 until the display reads less than ±5 digits.

5-14. Input Bias Current Null (R53).

a. Connect the Decade Resistance Box across the INPUT terminals. Select DC Function, .1V Range, and FILTER.

b. Allow instrument at least one hour warmup with covers in place.

c. Switch Decade Resistance Box between 0 and 1 Megohm. If display changes more than 50 digits as Decade box is switched, proceed to steps (d.) and (e.).

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

d. Remove top cover for access to R53, but keep cover in place when not adjusting R53.

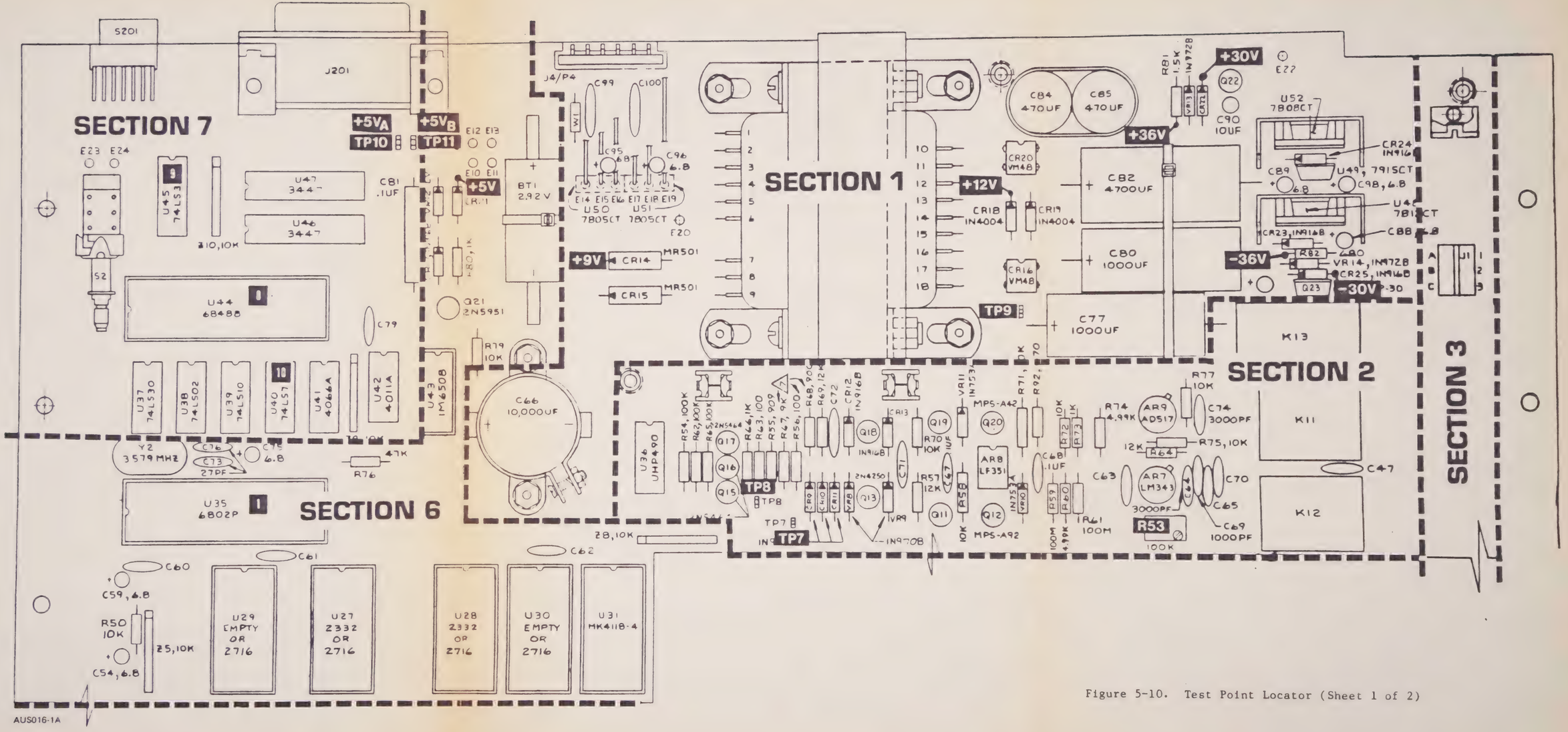


Figure 5-10. Test Point Locator (Sheet 1 of 2)

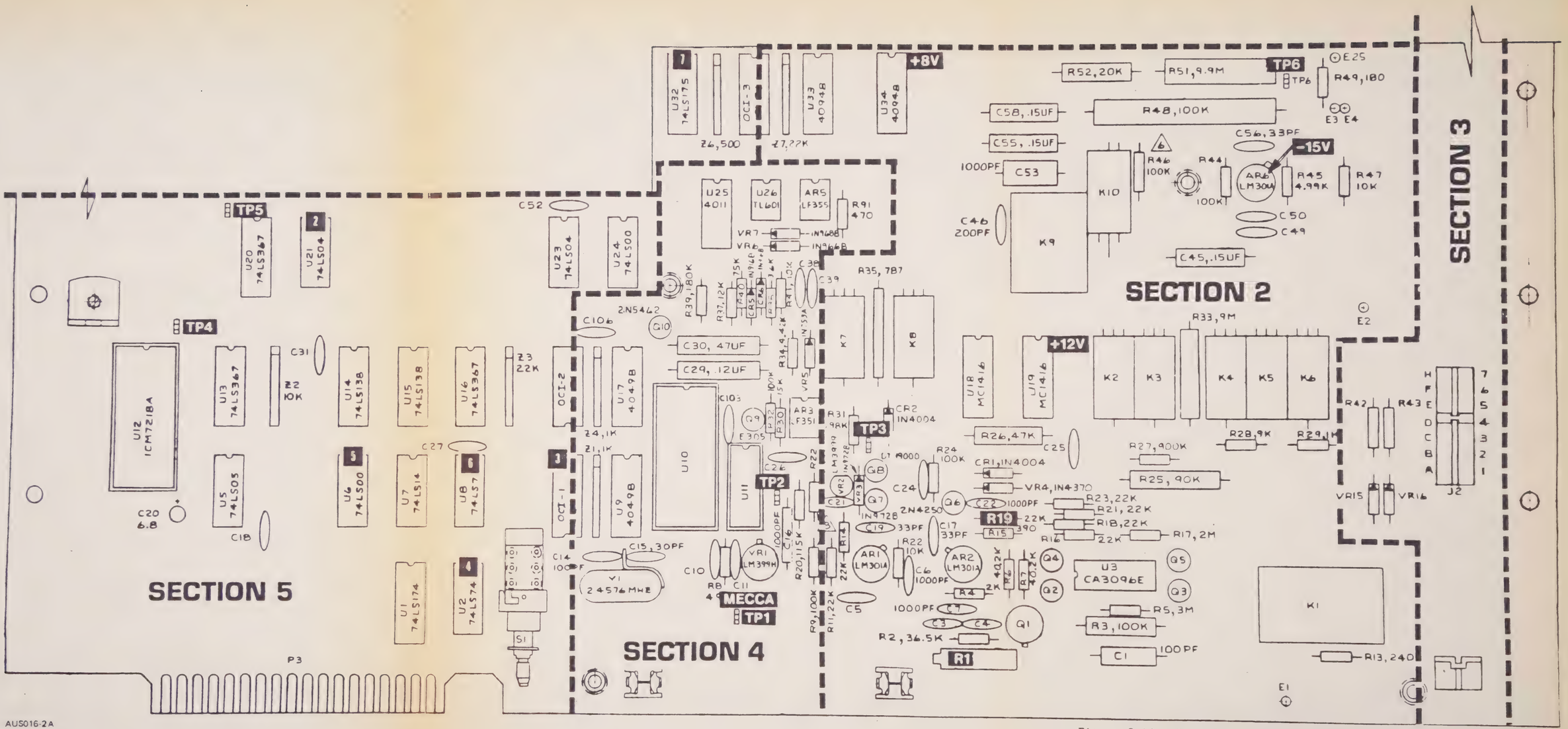


Figure 5-10. Test Point Locator (Sheet 2 of 2)

e. Adjust R53 until display changes less than ±50 digits as Decade box is switched between 0 and 1 megohm.

5-15. AC Converter Offset (R19).

a. Select AC function, 1V range.

b. Allow instrument at least one hour warmup with covers in place.

c. Apply 100 mV RMS at 400 Hz from the AC calibrator to the input HI and LO terminals.

d. Remove top cover warning on the AC converter plug-in module.

e. Adjust R19 on the AC Converter Plug-In Module for a minimum readout on the 5005 display.

5-16. Final Calibration.

5-17. Preliminary Setup.

a. Verify that all shields and covers are installed.

b. Short the INPUT terminals and GUARD terminal together.

c. Allow at least 2 hours warmup with covers installed before proceeding.

d. Select DC Function. Hold the .1V Range key depressed until "CAL 0" appears on the display, then release the Key.

e. Depress and hold the Calibration Switch.

f. Depress and release the RESET/NOMINAL Key.

g. Disable the Auto-range function by depressing the .1V Range Key. The AUTO annunciator will be off when disabled.

h. Refer to table 5-11 for the Function, Range, and Input for each calibration point. Verify that the AUTO annunciator remains off at each calibration point unless otherwise instructed.

5-18. 5 1/2 Digit Mode Calibration.

a. Connect the DMM to the Input Standard as specified for the first calibration point in table 5-11. Apply 0.00000 VDC to the DMM by dialing the Voltage Divider to zero.

b. Depress and hold the Calibration Switch.

c. If the average reading is not zero (4 digits p-p noise allowed), proceed to step (d); if equal to zero, release the Calibration Switch and proceed to step (f).

d. Increment or decrement the reading with the LOCAL/DOWN or SINGLE/UP keys or GPIB command until the reading is zero.

e. Release the Calibration Switch.

f. Connect the DMM to the Input Standard as specified for the next calibration point in table 5-11.

g. If the DMM reading is not equal to the Input Standard, proceed to step (h); if equal to the Standard, release the Calibration Switch and proceed to step (k.).

h. Depress and hold the Calibration Switch.

i. Increment or decrement the reading with the LOCAL/DOWN or SINGLE/UP keys (or GPIB Command) until the reading is equal to the Input Standard.

j. Release the Calibration Switch.

k. Repeat steps (f.) thru (j.) for each calibration point in table 5-11, except the 4 1/2 Digit Mode Scale Factor. At that step, see paragraph 5-19.

5-19. 4 1/2 Digit Mode Scale Factor Calibration.

a. Switch to the 4 1/2 Digit Mode (depress RESOL Key) and Auto-ranging (depress AUTO Key - verify that AUTO annunciator is ON).

b. Apply +1.0000 VDC and note reading.

c. Apply -1.0000 Vdc and note reading.

d. Depress and hold the Calibration Switch.

e. If the opposite polarity readings are equal in magnitude, but not equal to 1.0000, increment or decrement either polarity reading with the LOCAL/DOWN or SINGLE/UP Keys (or GPIB Command) until the readings are 1.0000.

f. If the opposite polarity readings are not equal in magnitude, increment or decrement either polarity reading until the readings are symmetrical around 1.0000 (e.g. -.9999 and +1.0001).

g. Release Calibration Switch.

5-20. Adjustments After Repairs. If major repairs are performed on the isolator, ohms amplifier, or AC converter, offset and bias adjustments associated with these circuits may need adjustment. Also, if repair work is performed in the vicinity of the non-volatile memory, or battery power is interrupted, the contents of the non-volatile memory may be invalidated.

5-21. Isolator Adjustment. Input Bias Current Null (R53) - See paragraph 5-14.

5-22. Ohms Amplifier Adjustment. Offset Zero (R1) - See paragraph 5-13.

5-23. Initializing Non-Volatile Memory:

a. Refer to table 5-12 for the Function, Range, and Input for each Non-Volatile memory calibration point.

b. At each point in the Table, set the DMM to the indicated Function and Range, and apply the specified input.

c. Depress and hold the Calibration switch.

d. While the Calibration switch is held depressed, press and release the RESET/NOMINAL key.

e. Release the Calibration switch.

5-24. AC Converter Hardware Calibration.

a. Perform the steps 1 and 2 that are listed in figure 5-11 after major repair to the AC Converter.

b. Perform steps 3 and 4 (figure 5-11) if the AC frequency response is not within the published specifications at 100 KHz after normal software calibration is performed (see paragraph 5-11).

c. Refer to figure 5-12 for the AC converter calibration point locations.

5-25. TROUBLESHOOTING.

5-26. General. To troubleshoot the voltmeter and track-down malfunctions it is necessary to be familiar with its normal operation. This manual is an important service tool, hence reading the complete manual is recommended.

A complete set of schematics for the DMM is contained in Section 6; the parts list is in Section 7.

The components, ICs and logic symbols used in the schematic diagrams are identical to those found in most manufacturers data sheets. Whenever a designator appears, the description follows immediately.

The drawing interconnects and continuations to other sheets are indicated in the following manner:

Plugs and Jacks: "P" indicates the plug or male section of the connector and J the jack or receptacle. P or J with the numbers from 1 to 99 are used on the mainframe or motherboard PCB locations, whereas P or J 100 series are on the front panel location and P or J 200 series represents the rear panel location. The E terminals are used for direct connection to the mainframe PC board.

5-27. Software Troubleshooting. Software and hardware problems may create the same symptoms but the cause may not be related. To isolate this problem, a list of General and Remote Error messages is supplied in table 5-14. The general error messages numbered 0 to 9 apply to local and remote operations. The messages numbered 10 to 13 apply to GPIB operation only.

Table 5-12. Calibration Points for Entry of Nominal Values Into Non-Volatile Memory

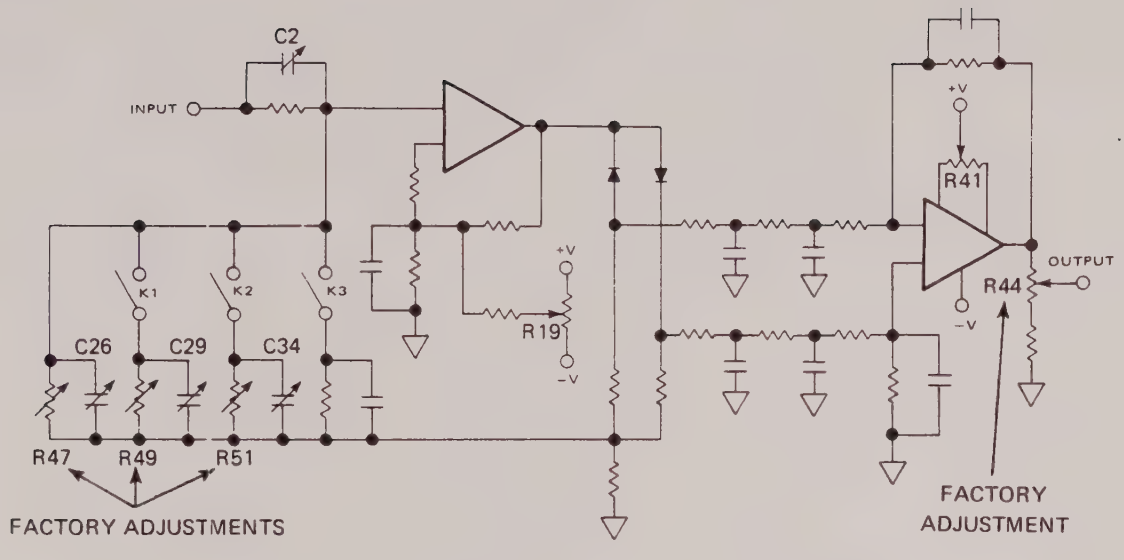
Function	Range	Input Standard (Note 1)
DC	.1V	0.0 VDC
	.1V	+0.1 VDC
	.1V	+0.1 VDC (Note 2)
	.1V	-0.1 VDC
	1V	+1.0 VDC
	1V	-1.0 VDC
	10V	+10 VDC
	10V	-10 VDC
	100V	+100 VDC
	100V	-100 VDC
	1 KV	+1000 VDC
	1 KV	-1000 VDC
AC	1 KV	0.0V RMS
	1V	1V RMS, 400 Hz
	10V	10V RMS, 400 Hz
	100V	100V RMS, 400 Hz
	1 KV	1000V RMS, 400 Hz
OHMS	100K	0.0
	.1K	100
	1K	1K L
	10K	10K
	100K	100K
	1000K	1M
	10,000K	10M

Note 1 - Unless otherwise noted, 10% accuracy is adequate.

Note 2 - Select 4 1/2 Digit mode (RESOL Key) and auto-ranging (AUTO Key) for this calibration only. Return to 5 1/2 Digit mode (RESOL Key), fixed range before continuing to the next step.

Table 5-13. Test Equipment

Item	Minimum Use Specification	Calibration Equipment
1. DC Power Supply	Adjustable 0-20 VDC	-
2. Oscilloscope	25 MHz Bandwidth	TEK 454
3. DMM	0.1% DCV	Racal-Dana 6000



AC CALIBRATION

1. Select AC, 1000V range. Short ± INPUT terminals. Adjust R41 for readout of all zeros. Remove short at input.

2. Set range to 1V; apply 100 mV at 400 Hz from AC calibrator. Adjust R19 for minimum readout. Recheck step 1.

3. Set calibrator to 20 kHz. Apply 1000 to the input and adjust C2 for a readout of 1000.00.

4. Change calibrator to 100 kHz. Apply inputs on each range as listed below. Adjust for proper readout.

Range	Input (RMS)	Adjust	Readout
1	1V	C26	1.00000
10	10V	C29	10.0000
100	100V	C34	100.000

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Figure 5-11. Averaging AC Calibration

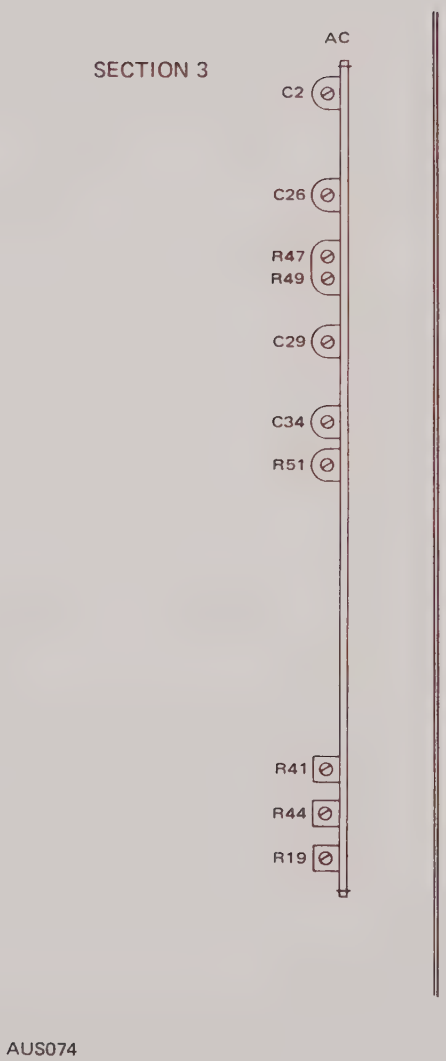


Figure 5-12. Calibration Points: AC Converter

5-28. Hardware Troubleshooting. To service hardware, it is important to know the normal operation of the DMM. The block diagram in figure 5-13 is presented as an overview to aid familiarization of the electrical configuration and figure 5-10 indicates the test point on the parts layout of the mainframe PCB assembly. The schematics in Section 6 complete the necessary details required to troubleshoot the voltmeter.

The DC voltages distributed throughout the DMM are a reliable status indicator and any deviation from normal can be readily observed. The normal voltages are supplied in table 5-15 for the major circuits on the PCB. The left column itemizes the names of the circuits and the instructions are listed across the top. The chart information progresses from left to right. Using the circuit listing 'DIGITAL SUPPLY' for example, it reads:

a. Required voltage column reads +5VA and +5VB.

b. Parts Layout Reference Column: A guide to test-point locations.

c. Meter Probe column specifies the test-point connection. It reads Positive TP10 and Negative common TP4.

The use of by-pass/decoupling capacitors is numerous through the PCB. A common location for these capacitors is at the Vcc input to a device. When voltage problems appear in a circuit, checking these capacitors first may reduce the search time.

5-29. Troubleshooting Performance Tests. The unit performance tests are designed to isolate a malfunction to a replaceable module or printed circuit board. In some cases where the printed circuit board is large and complex, the unit test is designed to isolate malfunction to a functional area of the board.

Both the unit and subassembly performance tests present test setup instructions, step by step instructions for monitoring the circuit under test and performance standards in the form of voltage levels or oscilloscope waveforms. For ease in locating the physical test point within the instrument, pictorial drawings are provided (Section 6).

Test points called out in the performance tests may be actual physical test points provided as convenient test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares or diamonds.

Note that the test points are numbered sequentially from the start of the performance tests and progress to the end. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to test point flags appearing on the assembly drawing in Section 6.

To perform subassembly performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage

Table 5-14. General and Remote Error Messages

Error Message No.	Error Message
	GENERAL ERROR MESSAGES
1	Not in the DC function, 0.1 range when zeroing the instrument.
2	Attempting to zero the instrument with an input voltage applied or to be input open-circuited. Connect a short across input terminals and repeat zero command.
3	The microprocessor's on-board RAM is defective (U35 on the motherboard).
4	The contents of the non-volatile memory have been disrupted, therefore the instruments calibration should be verified.
6	Attempted display of a number which is beyond 9.999E9, unlike the other error messages, Error 6 is always displayed on the front panel and never causes an SRQ to be sent to the controller, independent of whether the instrument is in local or remote.
7	The Model 5005 RAM is defective (U31 on the motherboard).
8	An attempt was made to store an overload reading to a register inside the DMM.
	GPIB ERROR MESSAGES
11	Triggered too fast or too often.
12	Syntax error during GPIB programming.

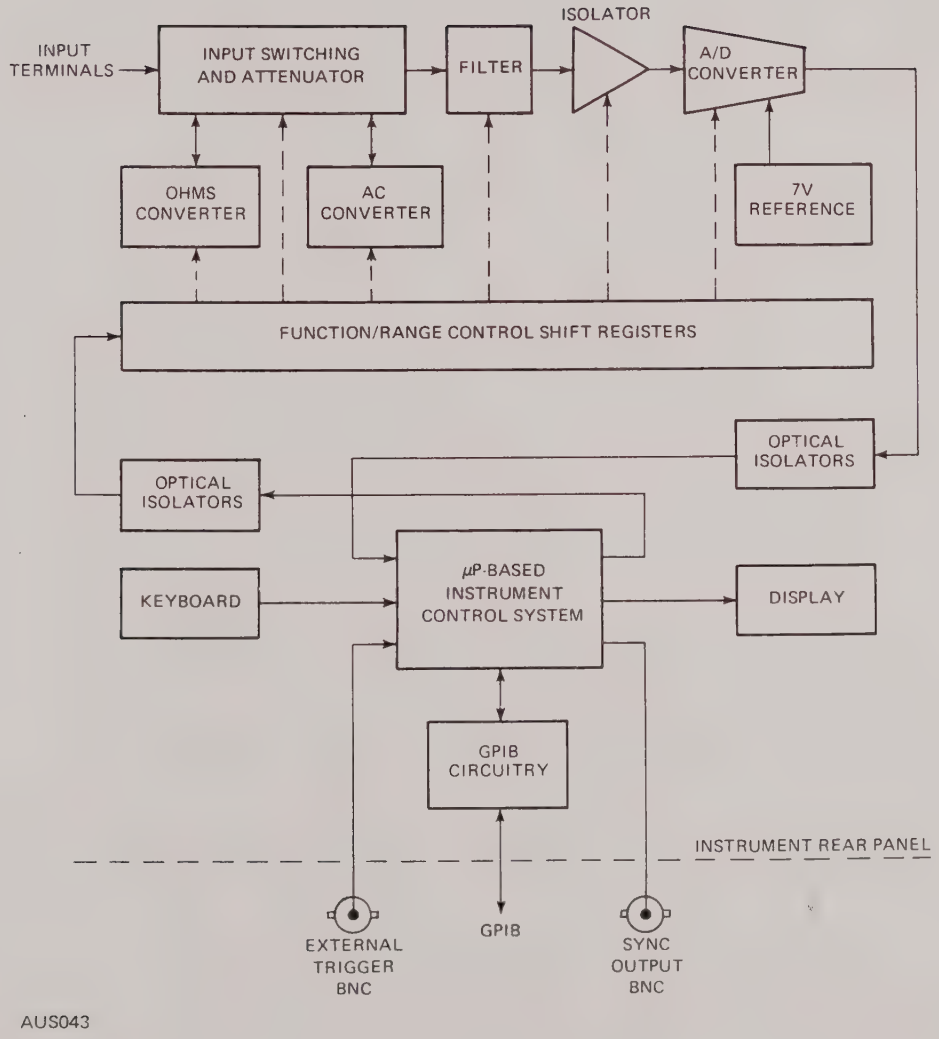


Figure 5-13. DMM Block Diagram

Table 5-15. Power Supply Voltage Checks (Schematic 431650-1)

Tests → / Circuit ↓	Required Voltage DC	Parts Layout Ref.	Meter Probes Pos. Neg.	Reading OK	Move Probe To →	Move Probe To →	Move Probe To →	AC Reading Change DMM Function
Digital Supply	+5VA	Fig. 5.4	Pos. TP10 Neg. TP4	No Next →	U50-IN No →	CR14, Cath. No →	→	Term 7 & 9 Power Trans.
	+5VB	Fig. 5.4	Pos. TP11 Neg. TP4	No Next →	U51-IN No →	CR15, Cath. No →	→	Term 7 & 9 Power Trans.
Non-Voltile Memory	+9V Un-Reg.	Fig. 5.4	Pos. CR14C Neg. TP4	No Next →	(Note: When +5VA or B OK, Then +9V OK) →			Term 7 & 9 Power Trans.
AC Converter Analog	+18V (+30V)	Fig. 5.4	Pos. J2-C Neg. TP9	No Next →	CR22, Cathode (+30V) No →	Lower Side R81 (+36V) No →	CR20+ (+36V) No →	Term 10 & 16 Power Trans.
AC Converter Analog	−18V (−30V)	Fig. 5.4	Pos. J2-3 Neg. TP9	No Next →	CR25, Anode (−30V) No →	Left Side of R82 (−36V) No →	CR20− (−36V) No →	Term 10 & 16 Power Trans.
Isolator	+36V Un-Reg.	Fig. 5.4	Pos. CR20+ Neg. TP9	No Next →	(Note: When +18V OK, Then +36V OK) →			Term 10 & 16 Power Trans.
	−36V Un-Reg.	Fig. 5.4	Pos. CR20− Neg. TP9	No Next →	(Note: When −18V, −30V OK, Then −36V OK) →			Term 10 & 16 Power Trans.
AC-DC Ohms	+12V Un-Reg.	Fig. 5.4	Pos. U19 Pin 16 Neg. TP9	No Next →	U48-IN No →	CR-16+ No →	→	Term 11 & 15 Power Trans.
Op-Amps	−15V	Fig. 5.4	Pos. Can AR6 Neg. TP9	No Next →	No → U49-IN	No → CR16−	→	Term 11 & 15 Power Trans
Relay Drive	+12V Un-Reg.	Fig. 5.4	Pos. CR18-Cath. Neg. TP9	No Next →	No →	No →	No →	Term 12 - 14 Power Trans.
A-D Converter	+8V	Fig. 5.4	Pos. U33 Pin 16 Neg. TP9	No Next →	U52-IN No →	→	→	Term 12 - 14 Power Trans.
Non-Voltile Battery	+3V	Fig. 5.4	Pos. BT1-Pos. Neg. TP4	No Replace				
DC Supply	+5V	Fig. 5.4	Pos. CR21-Pos. Neg. TP4	No Next →	Pos. CR14 Cath. +9V. No →	→	→	Terminals 7 & 9 Power Transformer

or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors, and capacitors in and around the area of malfunction.

Tables 5-16 and 5-17 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements.

WARNING

These servicing instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the instructions unless you are qualified to do so.

5-30. INTERFACE MAINTENANCE.

5-31. Fault Isolation. The self-test portion of the microprocessor uses the output line LEDs to display error messages. These LEDs are read in the same manner for errors as they are for data output. Each LED is weighted from 1 for CR 26 to 80,000 for CR 7, as follows:

80,000	8000	800	80	8
40,000	4000	400	40	4
20,000	2000	200	20	2
10,000	1000	100	10	1

The data outputs are all pure decimal, i.e., each decade has a value between 0 and 9. However, some error messages use the hexadecimal code, and evaluate as follows:

1	2	4	8	Value
-	-	-	-	0
X	-	-	-	1
-	X	-	-	2
X	X	-	-	3
-	-	X	-	4
X	-	X	-	5
-	X	X	-	6
X	X	X	-	7
-	-	-	X	8
X	-	-	X	9
-	X	-	X	A
X	X	-	X	B
-	-	X	X	C
X	-	X	X	D
-	X	X	X	E
X	X	X	X	F

Table 5-16. Digital Section Performance Test

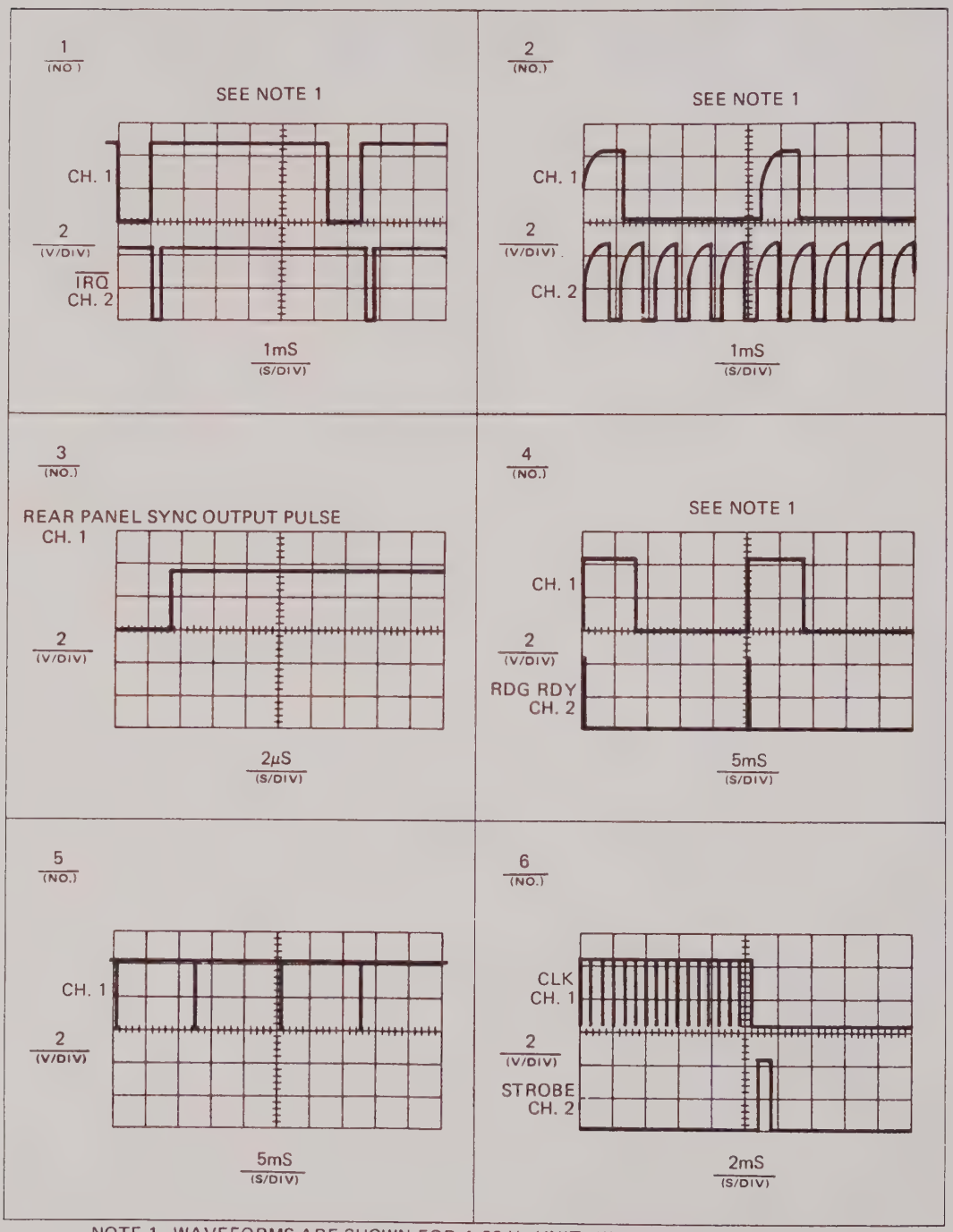
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Using conventional techniques, the Digital Section can only be tested to the point where certain "Knowns" can be verified. If the proper waveforms are not observed, the nearest Racal-Dana serivce center should be contacted.					
All measurements in this table are referenced to TP4, Digital Common. Power Switch: ON				Test Points Shown on Figure 5.4	
Disconnect any cables connected to Rear Panel GPIB and BNC Connectors	+5 VA +5 VA +5 VB $\overline{\text{Reset}}$ $\overline{\text{NMI}}$	U35 Pin 40 U35 Pin 6	1 1		+5V ± .25 VDC +5V ± .25 VDC +5V ± .25 V +2.5V to +5.25V with no excursions below +2.5V
Set Scope Trigger To Internal, Channel 1, + Slope	μP Clock E	U21 Pin 11	2		Waveforms #7, Ch. 1
	Inverse Signal $\overline{E}$	U21 Pin 10	2		Waveforms #7, Ch. 2
	Address Bus	U35 Pins 9 to 20 and 22 to 25	1		See Note Below
	Data Bus	U35 Pins 12 to 19	1		See Note Below
	VMA	U35 Pin 5	1		See Note Below
	R/$\overline{W}$	U35 Pin 34	1		See Note Below
	W/$\overline{R}$	U21 Pin 8	2		See Note Below
Scope Trigger Set To: Internal, + Slope, Channel 1	Digit Strobe Sync D6 (After Opto-isolation)	OCI1 Pin 11	3		Waveforms #2, Ch. 1
	1 KHz (After Opto-isolation) (approx. .83 KHz in 50 Hz Machine)	OCI1 Pin 14	3		Waveforms #2, Ch. 2

Note: These waveforms are asynchronous TTL signals. If the signals are always high or low at this point, it is an indication of a Fault.

Table 5-16. Digital Section Performance Test (Continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Instrument in "Hold" Mode (Press "SINGLE" Key on Keyboard) Scope Trigger Set To: Internal, – Slope, Channel 1	Clock to Interrupt - Control FF	U2 Pin 11	4		Waveforms #1, Ch. 1
	$\overline{IRQ}$ Input to μP	U35 Pin 4	1		Waveforms #1, Ch. 2
Instrument in "Hold" mode (Press "SINGLE" Key on Keyboard) Scope Trigger Set To: Internal, – Slope, Channel 1	$\overline{DSPE}$	U6 Pin 8	5		Waveforms #5, Ch. 1
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if required) Scope Trigger Set To: Internal, + Slope, Channel 1	$\overline{\text{End of Conversion}}$ (After Opto-isolation and Schmitt Trigger Inversion)	U8 Pin 11	6		Waveforms #4, Ch. 1
	Rdg Rdy (Reading Ready)	U8 Pin 9	6		Waveforms #4, Ch. 2
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if required)	Sync Output	Sync Output BNC (Rear Panel)	Rear Panel BNC		Waveform #3
Scope Trigger Set To: Internal, – Slope, Channel 1 Alternately Press "10" and "100" Range Keys at a Rapid Rate Scope Trigger Set To: Internal, + Slope, Channel 1	CLK	U32 Pin 7	7		Waveforms #6, Ch. 1
	Strobe	U32 Pin 2	7		Waveforms #6, Ch. 2

Table 5-16. Digital Section Performance Test (Continued)



NOTE 1 WAVEFORMS ARE SHOWN FOR A 60 Hz UNIT. WAVEFORMS TAKEN FROM A 50 Hz UNIT WILL BE 10% LOWER IN FREQUENCY.

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Table 5-16. Digital Section Performance Test (Continued)

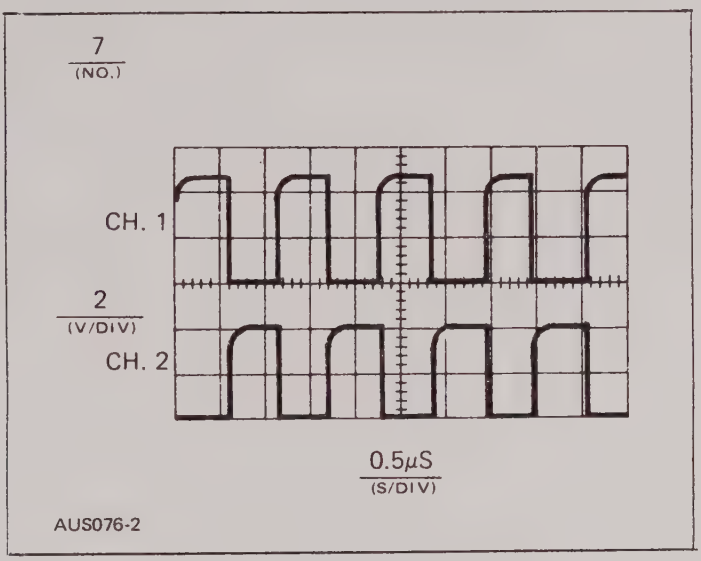

Table 5-17. GPIB Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Set All Rear Panel GPIB Switches to their Lower Position. Turn DMM's Power Off and then On again.	All measurements in this table are referenced to TP4, Digital Common.				
Disconnect all Cables from GPIB Connector	GPIB Data/Control Lines	J201 Pins 1-11 and Pins 13-17		Rear Panel Connector	+2.5 to +3.7V
	68488 GPIB I/O Lines	U44 Pins 16-23, Pins 25,26 Pins 29-36	8		+2.5 to +5.25V
DMM in "HOLD" Mode (Press "SINGLE" Key) Set Scope Trigger to Internal, – Slope, Channel 1	$\overline{ASE}$	U45 Pin 1 and/or Pin 15	9		GPIB Waveform # 1

Table 5-17. GPIB Performance Test (Continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
DMM set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if necessary) Talk Only (Set Rear Panel "talk only" Switch to "up" position) Set Scope Trigger to Internal, + Slope, Channel 1	Momentary Output Holdoff Pulse from μP (1 per Reading)	U39 Pin 8	10		GPIB Waveform # 2
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if necessary) Talk Only (Set Rear Panel "talk only" Switch to "up" position) Set Scope Trigger to Internal, + Slope, Channel 1	RFD	U44 Pin 18	8		GPIB Waveform # 3
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if necessary) Talk Only (Set Rear Panel "talk only" Switch to "up" position) Set Scope Trigger to Internal, + Slope, Channel 1	RFD $\overline{\text{GPIRQ}}$	U44 Pin 18 U44 Pin 40	8		GPIB Waveform # 4 Channel 1 GPIB Waveform # 4 Channel 2

Table 5-17. GPIB Performance Test (Continued)

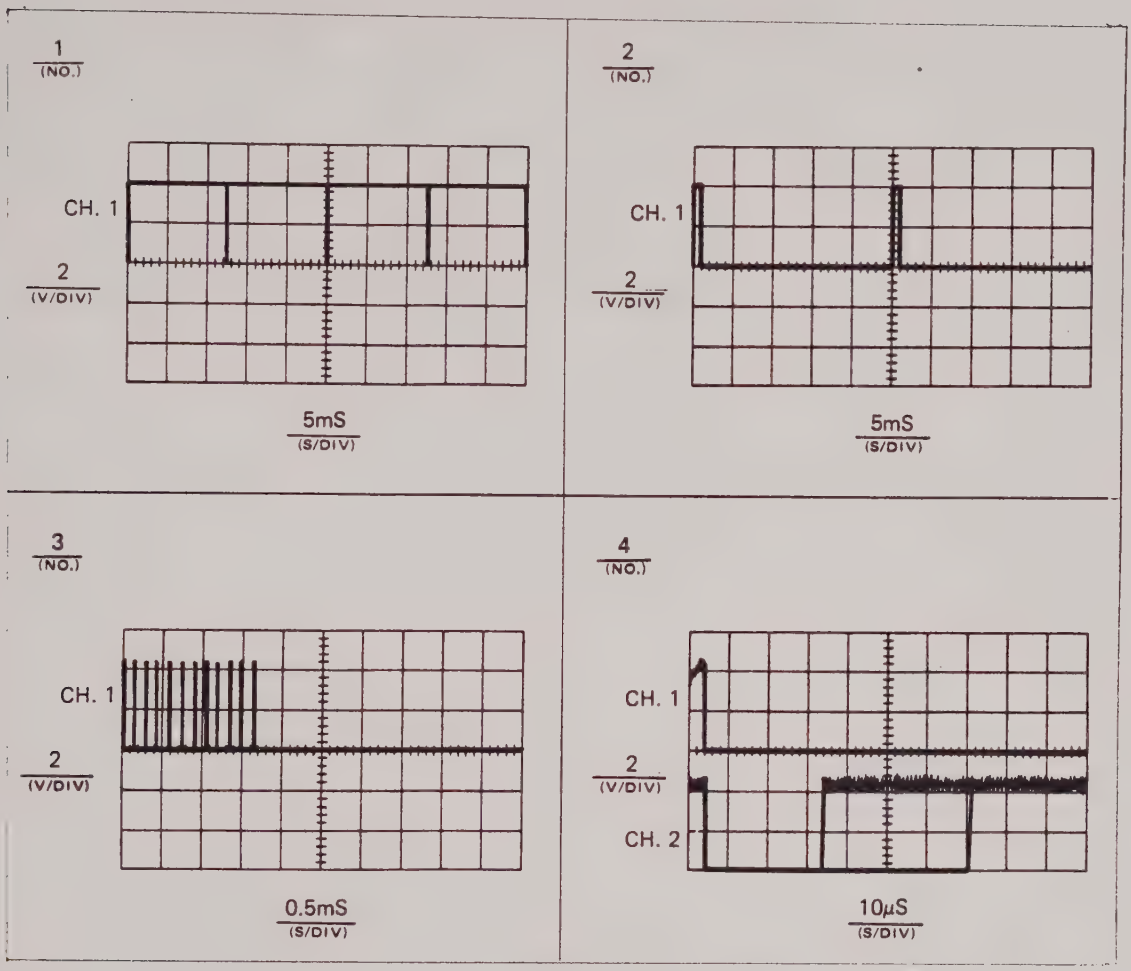

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Table 5-18. Digitizer Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
All measurements made in this table referenced to "Mecca" TP1. Instrument in 0.1V Range DC input shorted. Internal Trig. (Hit "Track" Key)	D1 - D5	U10 Pins 3-8			Waveforms # 2-6
Scope Trigger set to: Ch. 2, +, internal	D6	U10 Pin 8			Waveform # 1

Table 5-18. Digitizer Performance Test (Continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Instrument in 0.1V Range DC,input shorted. Internal Trig. (Press "Track" Key) Scope Trigger set to: Ch. 1, +, internal	1 KHz Clock	U10 Pin 28			Waveform # 7
Instrument in 0.1V Range DC. input shorted, internal trigger (Press "Track" Key) Scope trigger set to: Ch. 1, +, internal	2.5 MHz Clock	U10 Pin 14			Waveform # 8
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) Scope Trigger set to: Normal, +, internal	E.O.C.	U10 Pin 19			Waveform # 9
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) Scope Trigger set to: Normal, +, internal	M.Z.	U10 Pin 20			Waveform # 10
Instrument in 1V Range DC, +2V in internal trigger (Press "track" key) Scope Trigger set to: Normal, −, internal	M.Z. Switch	U26 Pin 4			Waveform # 11
Instrument in 1V Range DC, −2V in internal trigger (press track key) Scope trigger set to: Normal, +, internal	M.Z. Switch	U26 Pin 4			Waveform # 12
Instrument in .1V Range DC, input shorted, internal triggered (Press "track" key) + probe on: −probe on:		U11, Pin 10 Mecca TP-1			+7V ± 0.4V

Table 5-18. Digitizer Performance Test (Continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) + Probe on: –probe on:		 R34 eitherside Mecca TP-1			 –3.5V ± 1V

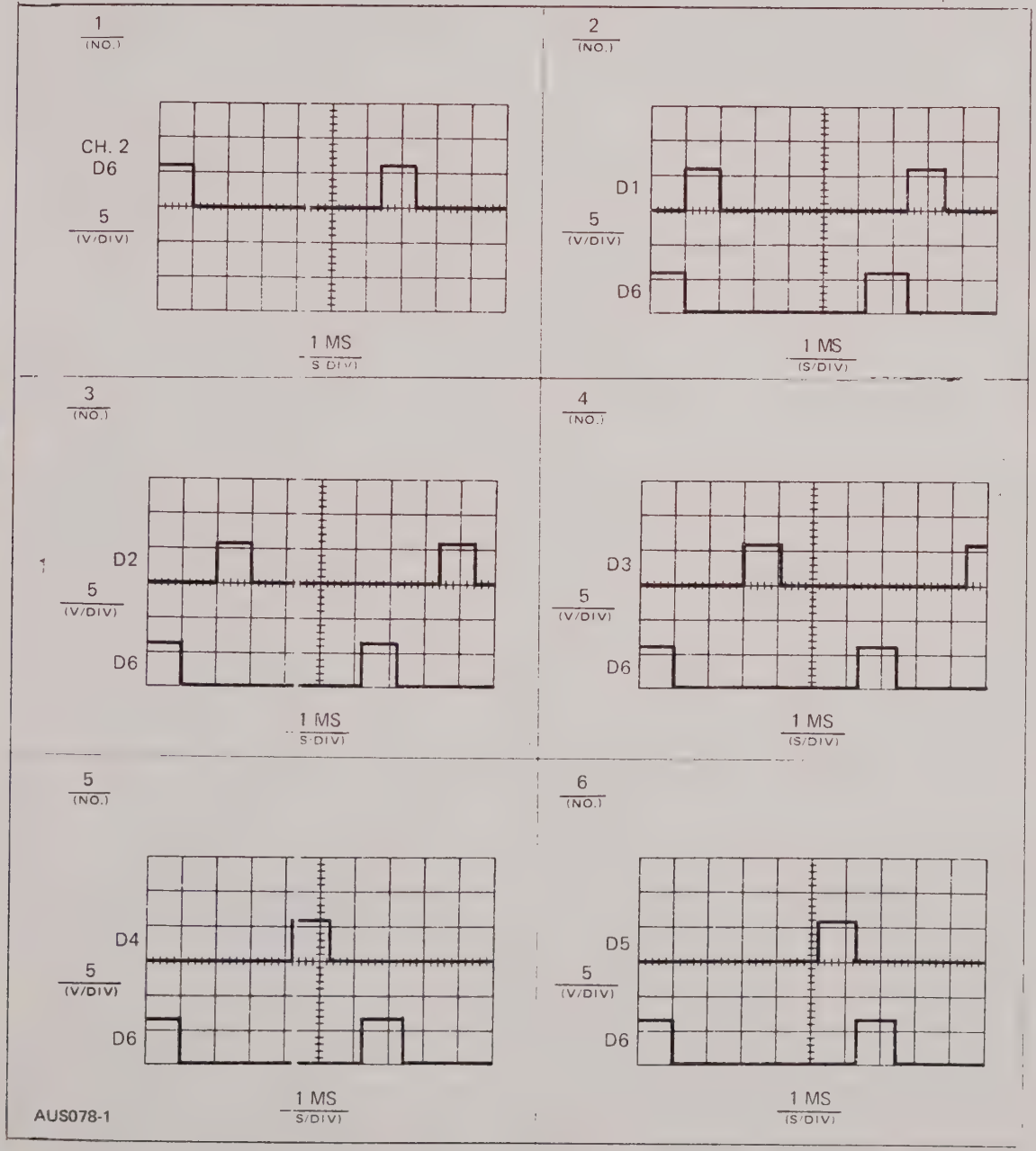
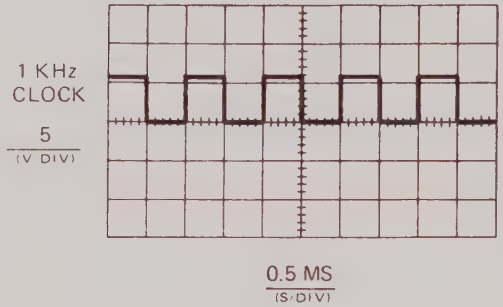
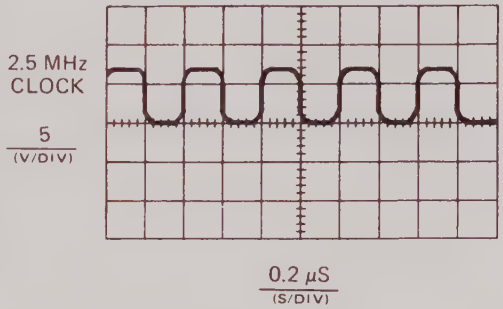


Table 5-18. Digitizer Performance Test (Continued)

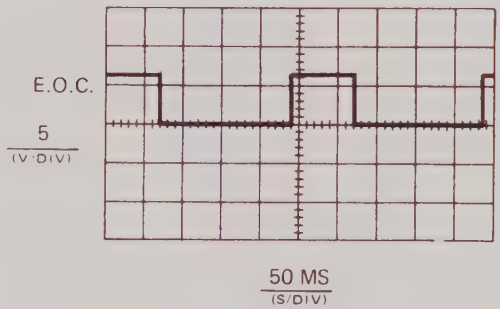
7 (NO.)



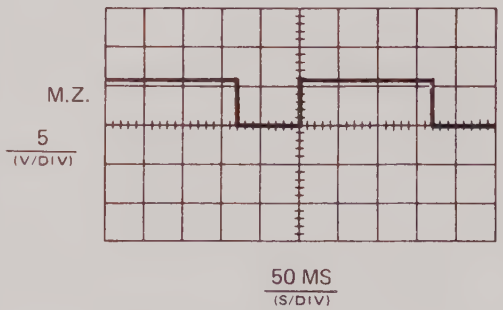
8 (NO.)



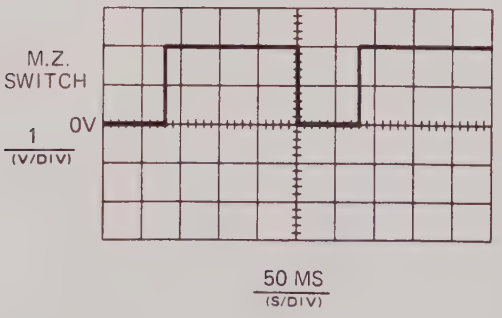
9 (NO.)



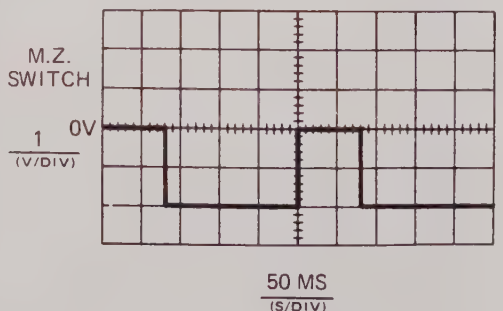
10 (NO.)



11 (NO.)



12 (NO.)



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5-32. Error Messages. All error messages are accompanied by the ERROR signal, resulting in a DMM BAL signal on DATAC.

Error 00011: No function found - It indicates that no function input was present when a rebalance or track command was issued. Remove the interface top cover assembly 3102505 before proceeding with error messages check.

WARNING

Removal of covers exposes potentially lethal voltages. Observe all Warning signs. Avoid contact with internal electrical connections while unit is connected to AC power.

a. Remove four phillips head screws from the top cover assembly.

b. Store the four screws for reinstallation of the top cover assembly.

c. Remove the 3102505 cover assembly.

d. Disconnect J3 on the rear of the interface assembly.

e. Disconnect W1 J1 on the PCB.

Depress ZERO OHM on front panel. If more than one LED illuminates simultaneously, read the indicated error number. If no error number arises, check function inputs. This error is self-resetting and may be generated by pressing 'REBAL' with no input from the test station.

Error 00012: No range found - It indicates that no range input was present when a rebalance or track command was issued. Depress and hold ZERO OHM, and momentarily depress RESET S1 on PCB. If more than one LED illuminates simultaneously, read the indicated error number and see directions for dealing with that error. If no error is indicated, check range input lines. Once error is cleared, a reset or a rebalance command will reset the system.

Error 99999: Overrange - This is precipitated by selecting a range which causes the interface to shift data more than 5 decimal places to the right. It is possible that the DMM display will not indicate an OL (overload) when this occurs due to the format of the data sent to the test station. Increasing the range or decreasing the input signal will resolve the error.

Error 00019: Invalid range - Invalid range results from the test station selecting a range that was not available on the CIMRON DVRM.

Error 00021: Line Feed not 14th character - Error 21 infers that the DMM has tried to send more than 14 characters to the interface. If a rebalance will not clear this error, turn off the DMM assembly for 10 seconds and turn it back on again. If the error recurs, check the DMM for a problem.

Error 00022: DMM generated error - This error is caused by the DMM not returning the full 14 character data string. The most likely cause of this is an error message from the DMM. This error message should be displayed on the DMM front panel.

IEEE-488 BUS ERRORS - These errors may result either from a loose or dirty bus connector at the rear of the DMM or the DMM power is not turned on.

Error 00033: No NRFD on talker - It is generated when the IEEE-488 bus from the DMM does not respond with an NRFD signal. If the interface board can be reset with the ZERO OHM button depressed and errors 00088 or 00089 do not occur, the problem is most likely in the DMM.

Error 00034: No NDAC on talker - It results from the interface not receiving an NDAC from the DMM when talking. If error 0008A or 0008B does not occur during a RESET - ZERO OHMS, the DMM probably is at fault.

Error 00035: No DAV on listener - The DMM did not respond with a DAV when sending data to the Interface. Check the bus wiring or the DMM for the difficulty if an error 00080 or 00081 does not result from a RESET - ZERO OHMS.

Error 00037: SRQ from DVM inconsistent - It is caused by the interface receiving an unexpected service request from the DMM. Push RESET - ZERO OHMS and look for error 8D which indicates that the interface is at fault, otherwise the bus or DMM produced the error.

Error 00036: No DAV (high) on listing - Interface did not receive cue to terminate listener handshake. Problem can be isolated to the DMM if a RESET - ZERO OHMS does not reveal error 00080 or 00081.

Error 00038: No SRQ after 2.5 seconds - DMM did not receive expected service request. If error 0008D occurs from a RESET - ZERO OHMS, the fault is located either on the interface board or the bus wiring.

After completion of the Error Messages check, reassemble the DMM interface as follows:

a. Reconnect W1 J1 on the PCB.

b. Reconnect J3 on the rear of the interface assembly.

c. Reinstall the 3102505 cover assembly.

d. Secure the cover assembly with the four phillips screws removed from the cover.

5-33. Interface Hardware Error.

Error 00041: Bad RAM - Replace random access memory IC (U46).

INTERFACE INPUT/OUTPUT ERRORS: The errors only occur after a RESET - ZERO OHMS. They indicate that a fault exists in the input/output circuits and can be used to track down faulty wiring and ICs by working from the input or output pin towards the center of the board. Opposite each of the following error numbers lies the associated output pin on the interface board.

FUNCTION INPUTS	VALUE	J3 PIN NUMBER
MV	00050	49
AC	00051	47
KOHM	00052	45
+ RATIO	00053	43
- RATIO	00054	41
DC	00055	39
TRACK	00056	37
REBAL	00057	35

RANGE INPUTS	HEX VALUE	J3 PIN NUMBER
1 (A)	00060	50
10 (B)	00061	48
100 (C)	00062	46
1000 (D)	00063	44
10,000 (E)	00064	42
NO INPUT	00065	40
SENSITIVITY 1	00066	38
FILTER	00067	36

5-34. IEEE Data Line Errors.

DATA LINE	ERROR VALUE	PIN NO.	IC
DI01 FAILED LOW (HIGH)	00070 (71)	2	U54
DI02 FAILED LOW (HIGH)	00072 (73)	7	U54
DI03 FAILED LOW (HIGH)	00074 (75)	15	U54
DI04 FAILED LOW (HIGH)	00076 (77)	9	U54
DI05 FAILED LOW (HIGH)	00078 (79)	2	U53
DI06 FAILED LOW (HIGH)	0007A (7B)	7	U53
DI07 FAILED LOW (HIGH)	0007C (7D)	15	U53
DI08 FAILED LOW (HIGH)	0007E (7F)	9	U53

5-35. IEEE Control Line Errors.

DATA LINE	ERROR VALUE	PIN NO.	IC
DAV FAILED LOW (HIGH)	00080 (81)	2	U48
ATN FAILED LOW (HIGH)	00082 (83)	7	U48
IFC FAILED LOW (HIGH)	00084 (85)	15	U48
REM FAILED LOW (HIGH)	00086 (87)	9	U48
NRFO FAILED LOW (HIGH)	00088 (89)	2	U47
NDAC FAILED LOW (HIGH)	0008A (8B)	7	U47
EOI FAILED LOW	0008C	9	U47
SRQ FAILED LOW	0008D	15	U47

5-36. Print Control Outputs.

POLARITY FAILED LOW (HIGH)	00090(94)
PRINT FAILED LOW (HIGH)	00091(95)
ERROR FAILED LOW (HIGH)	00092(96)
OVERRANGE FAILED LOW (HIGH)	0093(97)

Print control errors indicate a failure of an I/O port of U46.

5-37. Output Check. Remove the interface top cover assembly 3102505 before proceeding with the output check.

WARNING

Removal of covers exposes potentially lethal voltages. Observe all Warning signs. Avoid contact with internal electrical connections while unit is connected to AC power.

a. Remove four phillips head screws from the top cover assembly.

b. Store the four screws for reinstallation of the top cover assembly.

c. Remove the 3102505 cover assembly.

d. Disconnect J3 on the rear of the interface assembly.

e. Disconnect W1 J1 on the PCB.

While holding the ZERO OHMS switch depressed, depress the RESET switch S1 on the PCB and then release. As long as the ZERO OHMS switch is held depressed, the output LEDs will sequence from 1 to 80,000. This verifies the operation of each output line up to the LED. Releasing the ZERO OHM switch will complete the self-test portion of the program.

f. Reconnect W1 J1 on the PCB.

g. Reconnect J3 on the rear of the interface assembly.

h. Reinstall the 3102505 cover assembly.

i. Secure the cover assembly with the four phillips screw removed in step (a).

5-38. DISASSEMBLY OF DIGITAL MULTIMETER ASSEMBLY.

5-39. General.

The following paragraphs provide step-by-step instructions for disassembly of the Test Set Digital Multimeter (DMM) assembly.

NOTE

Retain all hardware removed during disassembly.

5-40. Procedures. Disassemble the DMM as follows:

a. Turn off power to the Test Set at the circuit breaker.

b. Remove any external connections to the DMM front panel.

c. Remove four screws securing the DMM drawer assembly to the Test Set.

d. Slide drawer out approximately 4 inches, loosen and remove ground strap bracket from left side of drawer. Leave the ground strap attached to the cabinet.

e. Slide drawer forward until it latches.

f. Depress latches on drawer slides and pull drawer forward until the cables at the rear of the chassis can be reached.

g. Disconnect four plugs from J1, J2, J3, and J4 at the rear of the chassis.

h. Remove locking pin from rear of DMM cable control arm on station left rail assembly.

i. Pull drawer from cabinet and install on bench.

j. Remove six screws securing two slides to drawer (see figure 5-14). Remove slides.

k. Remove four screws from rear cover (labeled DANGER - 120 VOLTS) (see figure 6-8).

l. Disconnect power cable from receptacle POWER on rear of DMM and from receptacle J5 on the interior of the drawer.

m. Release two captive screws securing plug P2 to IEEE-STD-488 PORT on back of DMM, and remove plug.

CAUTION

In next step, use care in pulling plug P1. The DMM Interface PC card is not secured in this area, and can be broken.

n. Release two spring latches securing plug P1 to J1 on the PC card, and remove plug and cable W1.

o. Remove, identify and tag 5 banana plugs from back panel of DMM.

p. Remove ground strap bracket.

q. Remove 8 screws securing DMM to drawer (see figure 5-14). Lift DMM out of drawer.

r. Remove 8 screws (with 4 washers each) securing 2 filler plates to DMM. Remove filler plates.

s. Remove 4 screws, 4 flatwashers, 4 lockwashers, 4 nuts and 4 ground wires from J6. Remove J6 from front panel.

t. Unsolder and tag leads from REBAL switch S2. Compress mounting fingers on rear of S2, and pull S2 out through front of panel.

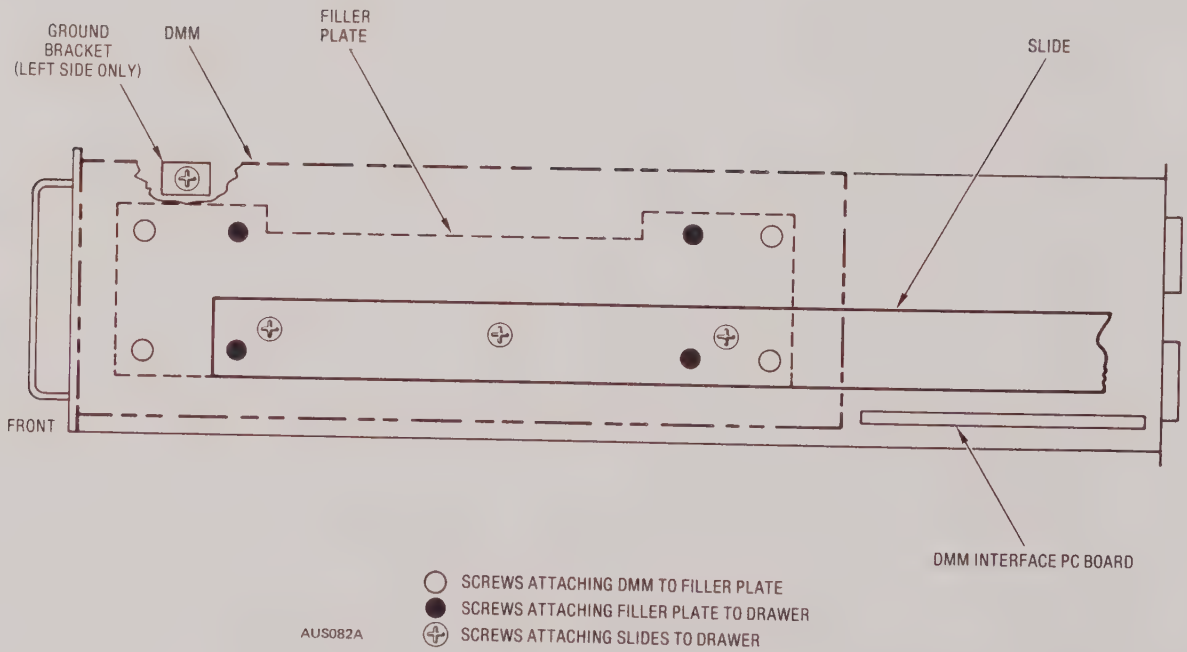


Figure 5-14. DMM Assembly to Drawer

u. Unsolder and tag leads from ZERO OHM switch S1. Compress mounting fingers on rear of S1, and pull S1 out through front of panel.

v. Unsolder and tag 2 leads (red and white) from LOAD side of EMI FILTER FL1.

w. Unsolder and tag 3 leads (red, white, shield) from LINE side of EMI FILTER FL1.

x. Remove two 8-32 screws, 2 lockwashers, and 2 nuts from EMI FILTER. Remove filter FL1.

y. Remove four 6-32 screws, 4 lockwashers, and 4 nuts from receptacle J2. Remove receptacle from panel.

z. Unsolder and tag 2 wires from circuit breaker CB1 on the front panel.

aa. Remove 1/2 inch nut from CB1 and remove CB1 from front panel.

ab. Remove four 6-32 screws, 4 lockwashers, and 4 nuts from receptacle J5. Remove J5 from panel.

NOTE

J3 and J4 are wire-wrapped connectors, as are the terminals on the DMM Interface PC board. Handle with care. Do not disconnect J3 or J4 from DMM Interface PC board.

ac. Remove four 6-32 screws, 4 lockwashers, and 4 nuts from J3. Remove J3 from panel.

ad. Remove four 6-32 screws, 4 lockwashers, and 4 nuts from J4. Remove J4 from panel. No further disassembly of connectors is recommended unless connectors have been damaged.

ae. Remove two 10-32 screws from bracket holding power supply to the rear panel.

af. Carefully turn the power supply until access is possible to the leads attached to the terminal board.

ag. Unsolder and tag 4 leads (red and white) from transformer T1.

ah. Unsolder and tag 6 leads from terminal board on power supply.

ai. Remove power supply. No further disassembly is required or recommended unless the power supply is malfunctioning.

aj. Remove 7 screws securing DMM Interface PC board to bottom of drawer. Remove PC board.

ak. This completes the disassembly of the DMM assembly.

5-41. REASSEMBLY OF DIGITAL MULTIMETER ASSEMBLY

5-42. General.

The following paragraphs provide step-by-step instructions for assembly of the Test Set DMM assembly.

NOTE

Reinstall all wires as previously tagged during disassembly.

5-43. Procedures. Assemble the DMM as follows:

a. Verify that power has been removed from the Test Set.

b. Position DMM Interface PC board in the bottom rear of drawer, and secure with 7 screws (see figure 6-10).

c. Position 5 VDC power supply XM 15-5 inside the rear of right drawer.

d. Solder 6 leads to terminal board (see figure 6-9) on power supply.

e. Solder 4 leads to terminals of transformer T1 on power supply. (Red lead to terminal 3, white lead to terminal 1). See figure 6-9.

f. Carefully turn the power supply until the holes in the mounting bracket are aligned with the holes in the rear of the drawer (power transistors face inboard). See figure 6-8, sheet 2. Secure the bracket to the drawer using two 10-32 screws.

g. Insert receptacle J4 into rear panel and secure with four 6-32 screws, 4 lockwashers, and 4 nuts. Use care not to stress pin connectors on J4 or the PC board.

h. Insert receptacle J3 into rear panel and secure with four 6-32 screws, 4 lockwashers, and 4 nuts. Use care not to stress pin connections on J3 or PC board.

i. Insert J5 into rear panel and secure with four 6-32 screws, 4 lockwashers, and 4 nuts.

j. Insert circuit breaker CB1 into front panel and secure with 1/2 inch nut.

k. Solder 2 wires to terminals of circuit breaker CB1. See figure 6-9.

l. Insert receptacle J2 into rear panel and secure with four 6-32 screws, 4 lockwashers, and 4 nuts.

m. Attach EMI FILTER FL1 to rear panel using two 8-32 screws, 2 lockwashers, and 2 nuts.

n. Solder 3 leads (red, white, and shield) to the terminals on the LINE side of EMI FILTER FL1. See figure 6-9.

o. Solder 2 leads (red and white) to the terminals on the LOAD side of EMI FILTER FL1. See figure 6-9.

p. Position ZERO OHM switch S1 in cutout in front panel, and snap into place.

q. Solder 2 leads to S1 as shown in figure 6-9.

r. Position REBAL switch S2 in cutout in front panel, and snap into place.

s. Solder 2 leads to S2 as shown in figure 6-9.

t. Insert receptacle J6 in front panel and secure with 4 screws, 4 flatwashers, 4 lockwashers, and 4 nuts, and secure 4 ground wires.

u. Install filler plates on either side of DMM using 8 screws. See figure 5-14 for placement.

v. Insert DMM into drawer and secure with 8 screws as shown in figure 5-14.

w. Install drawer slides and secure with 6 screws (see figure 5-14).

x. Insert 5 banana plugs into jacks on rear panel of DMM (see figure 6-9).

y. Engage plug P1 of cable W1 to J1 on the DMM Interface PC card and secure with the attached 2 spring latches.

z. Attach plug P2 of W1 to the IEEE-STD-488 PORT on the back of the DMM and secure with the 2 captive screws on P2.

aa. Connect power cable to receptacle J5 on the interior of the drawer, and the other end to receptacle POWER on rear of DMM.

ab. Install rear cover on drawer and secure with 4 screws.

ac. Lift drawer (DMM assembly) into position in test set and engage the slides.

ad. Connect 4 plugs to J1, J2, J3, and J4 at the rear of the DMM drawer.

ae. Connect ground strap from cabinet to left side of drawer using ground strap bracket.

af. Install locking pin on rear of DMM cable control arm on station left rail assembly.

ag. Push drawer into cabinet all the way, and secure with 4 front panel screws.

6. DRAWINGS

6-1. DRAWINGS

6-2. This section contains assembly drawings and schematic diagrams for the digital multimeter and interface assembly. Table 6-1 lists the drawings peculiar to the RACAL-DANA digital multimeter. Table 6-2 lists General Dynamics Electronics drawings which describe the mechanical and electrical interfaces between the multimeter and the F-111 Test Station.

Table 6-1. Drawing Index

FIGURE	DRAWING	TITLE	PAGE
6-1	404104 "1"	DMM Chassis Assembly	6-3
6-2	401651 "1"	DMM Display, PCB Assembly	6-5
6-3	431651 "1"	DMM Display Schematic	6-7
6-4	401650 "A"	DMM Motherboard, PCB Assembly (Sheet 1 and 2)	6-9
6-5	431650 "A"	DMM Motherboard, Schematic (Sheet 1 thru 11)	6-13
6-6	404107 "A"	DMM AC Converter, PCB Assembly	6-35
6-7	432131 "A"	DMM AC Converter, Schematic	6-37

Table 6-2. Drawing Index

FIGURE	DRAWING	TITLE	PAGE
6-8	3102494	Digital Multimeter Mod Assembly (Sheet 1 and 2)	6-39
6-9	3102570	Digital Multimeter Mod Interconnection Diagram	6-43
6-10	3102498	Interface Circuit Card Assembly	6-45

Table 6-2. Drawing Index- Continued

FIGURE	DRAWING	TITLE	PAGE
6-11	3102499	Interface Circuit Card Schematic Diagram	6-47
6-12	3102505	DMM Interface Cover	6-49
6-13	3102519	Interface Cable W1 Assembly	6-51
6-14	XM-15-5	Interface Power Supply Schematic Diagram	6-53

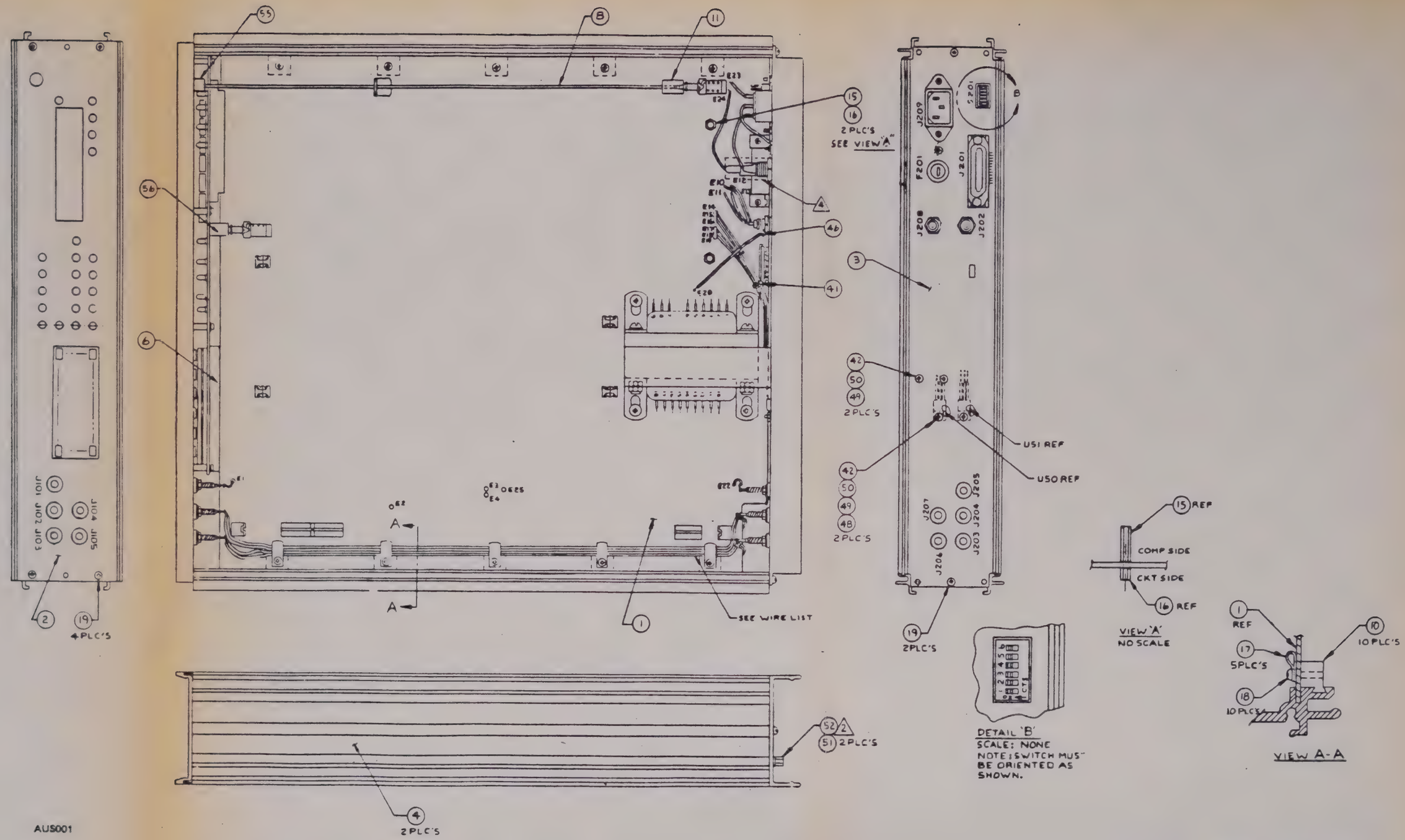
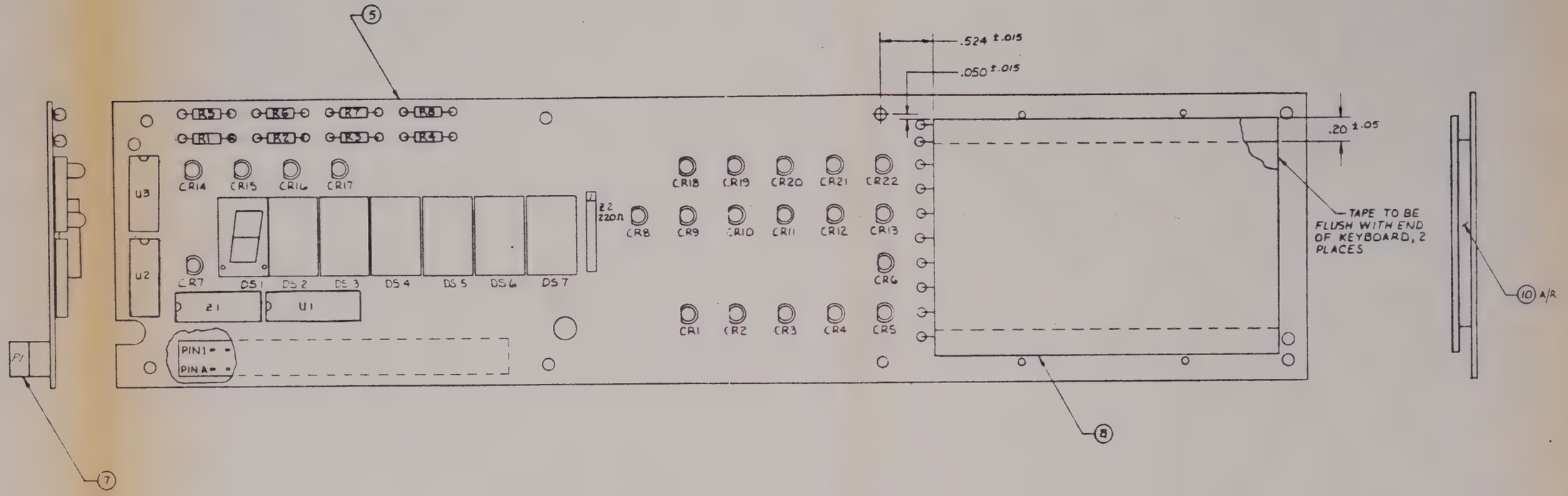


Figure 6-1. DMM Chassis Assembly
(404104 "1")



2. ALL RESISTORS ARE 4.3Ω, ¼W, 5%.

1. SCHEMATIC REFERENCE 431651

NOTES: UNLESS OTHERWISE SPECIFIED

AUS002

Figure 6-2. DMM Display, PCB Assembly (401651 "1")

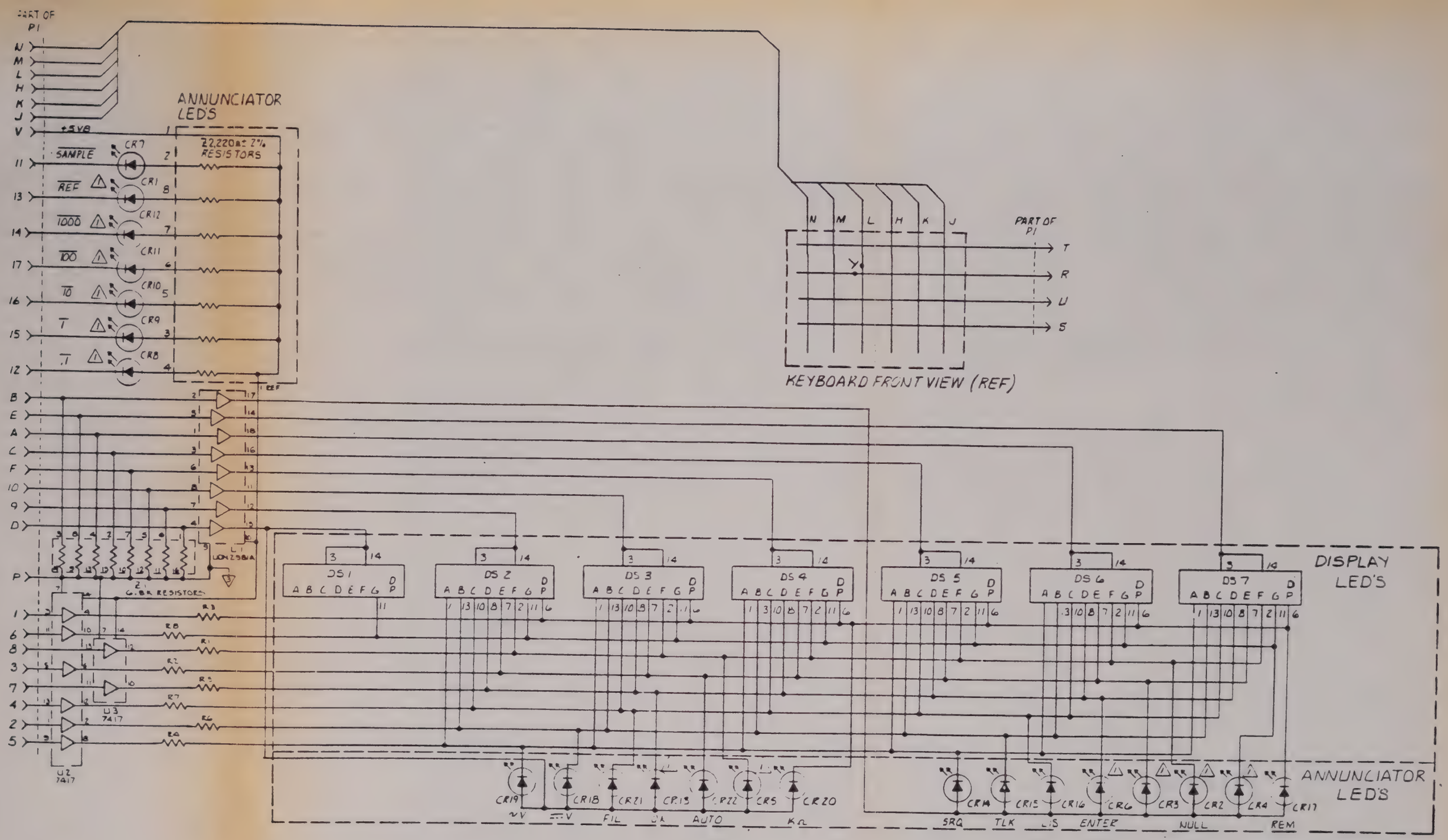


Figure 6-3. DMM Display Schematic (431651 "1")

3 CR1 THRU CR22 ARE 210072.

2 DS1 THRU DS7 ARE 210074.

1 R1-R8 ARE 4.3Ω 1/4W 5%.

AUS003

NOTE UNLESS OTHERWISE SPECIFIED
1. ASSEMBLY PROCESSES & PROCEDURES TO CONFORM TO GOOD WORKMANSHIP STANDARDS.
2. REFERENCE SCHEMATIC NO 431650
3. RESISTORS ARE IN OHMS
4. CAPACITORS ARE IN UF, 01
5. BEND TABS 90° ON FARSIDE OF PCB.
6. PART OF RESISTOR SET 012065.
7. PART OF RESISTOR SET 012063.
8. PART OF RESISTOR SET 012064.
9. TRANSISTORS ARE 200200.

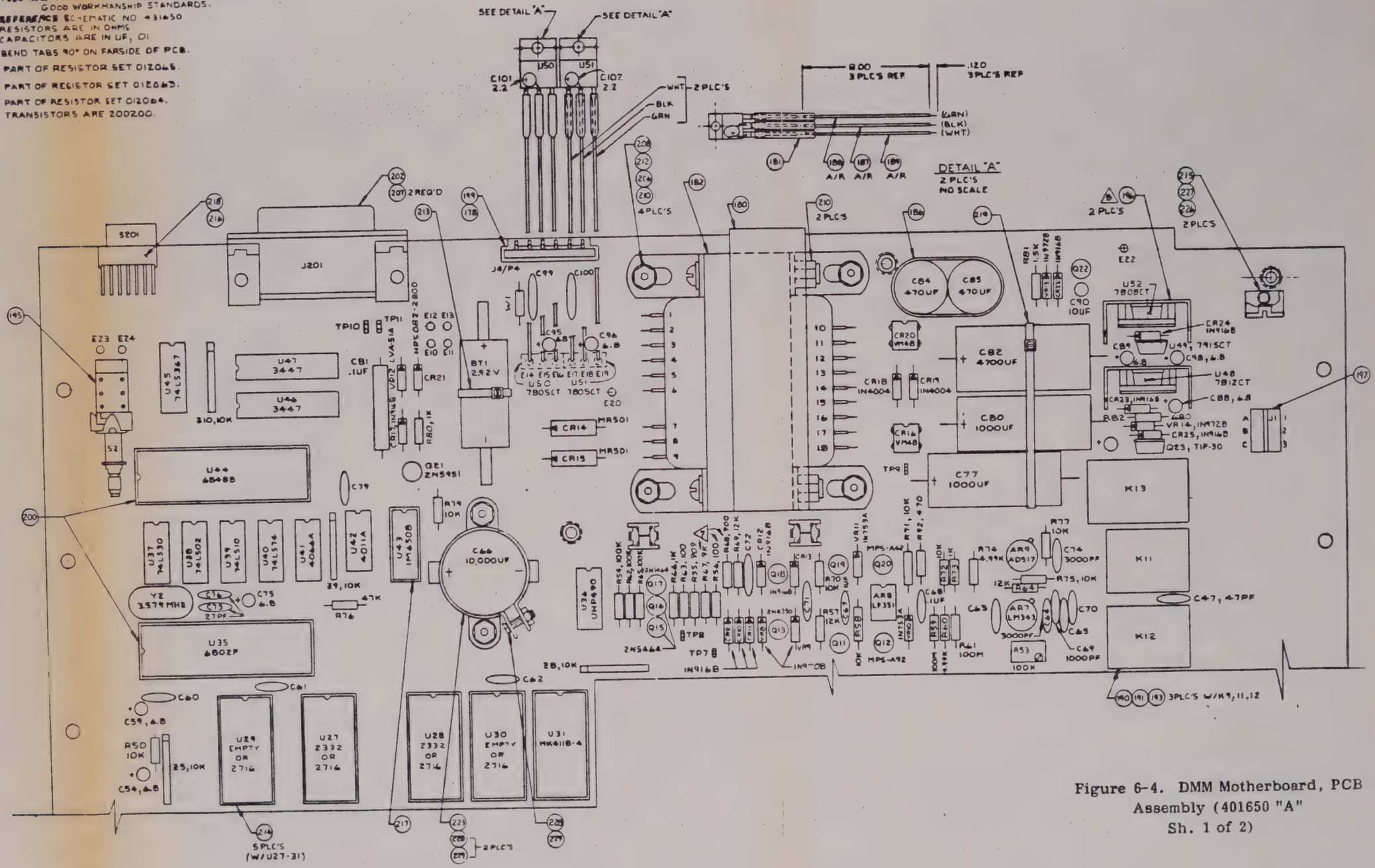
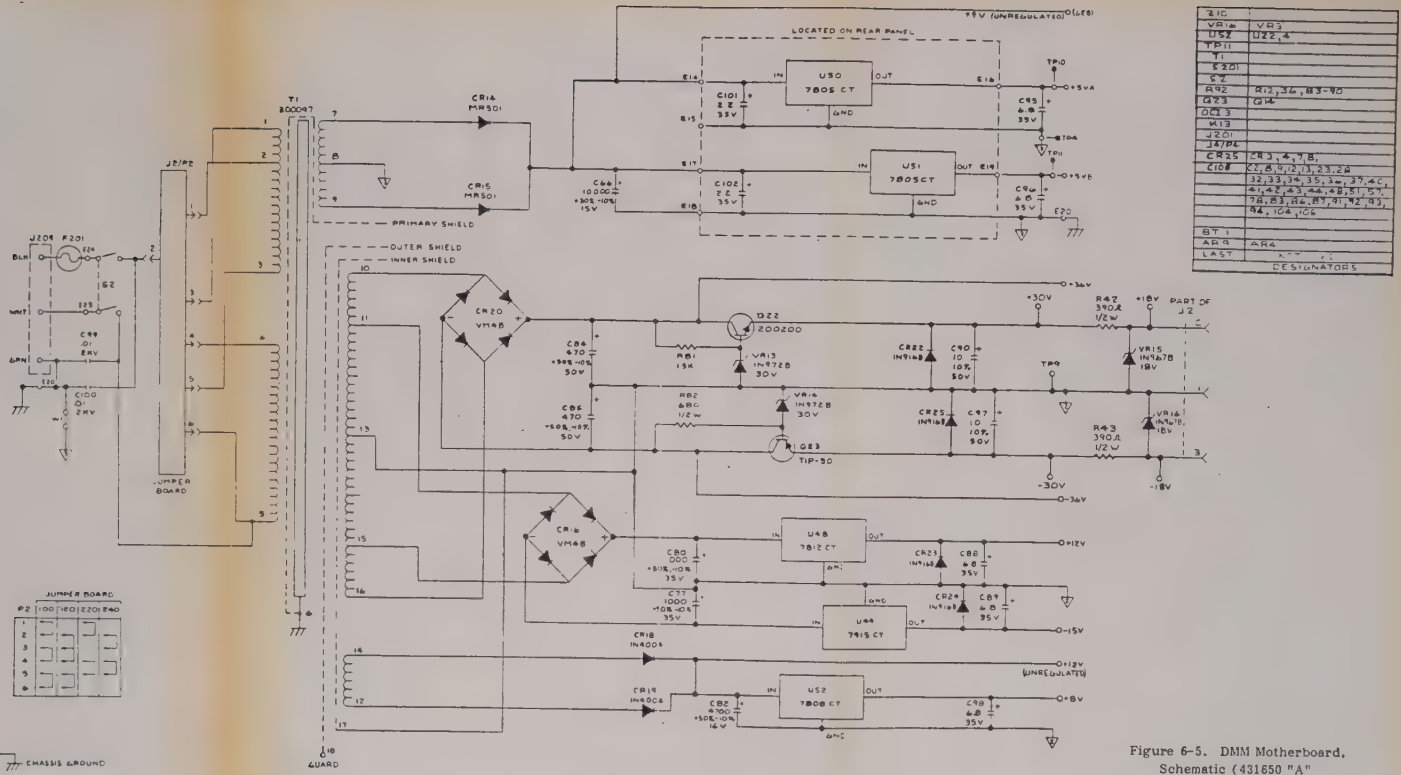


Figure 6-4. DMM Motherboard, PCB Assembly (401650 "A" Sh. 1 of 2)



Z1C	
VR16	VR3
U52	U22,4
TP11	
T1	
S201	
S2	
A92	R12,36,83-90
Q23	Q14
OC13	
W13	
J201	
J4/P4	
CR25	CR3,4,7,8,
C108	C2,8,9,12,13,23,28
	32,33,34,35,36,37,40
	41,42,43,44,48,51,57,
	78,83,86,87,91,92,93,
	94,104,105
BT1	
AR9	AR4
LAST	

DESIGNATORS

JUMPER BOARD

P2	100	160	220	240
1				
2				
3				
4				
5				
6				

3 RESISTOR NETWORKS ±2%.
2 CAPACITORS ARE IN MF, ±20%, 100V
1 RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES UNLESS OTHERWISE SPECIFIED FOR PAGES 1-

Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 1 of 11)

6-13/6-14

205
207
192
2 PLC'S
(w/U10, U12)
198
11 PLC'S
TP1 THRU TP11
TP5
U20
74LS367
U21
74LS04
TP4
C31
R2
10K
U13
74LS367
U12
ICM7218A
U5
74LS05
C20
6.8
C18
P3
177

AUS004 2

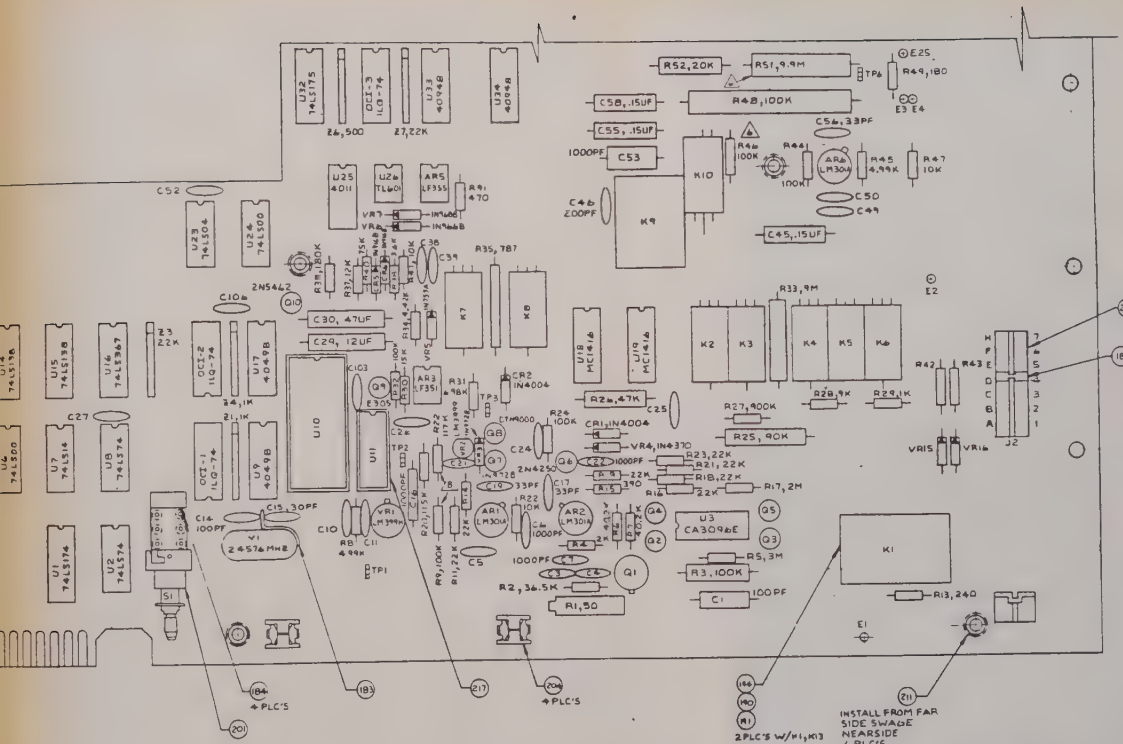


Figure 6-4. DMM Motherboard, PCB Assembly (401650 "A" Sh. 2 of 2)

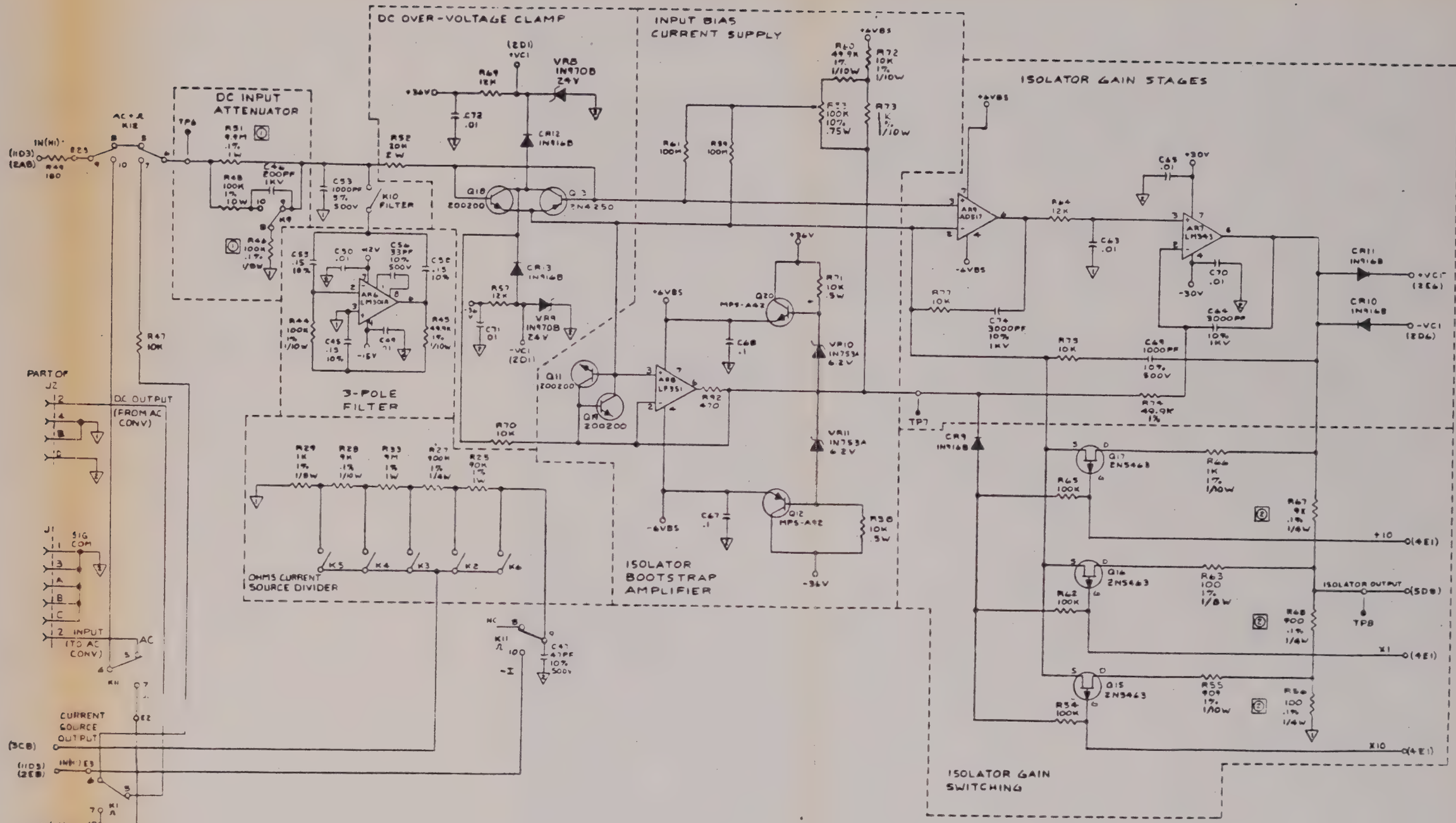


Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 2 of 11)

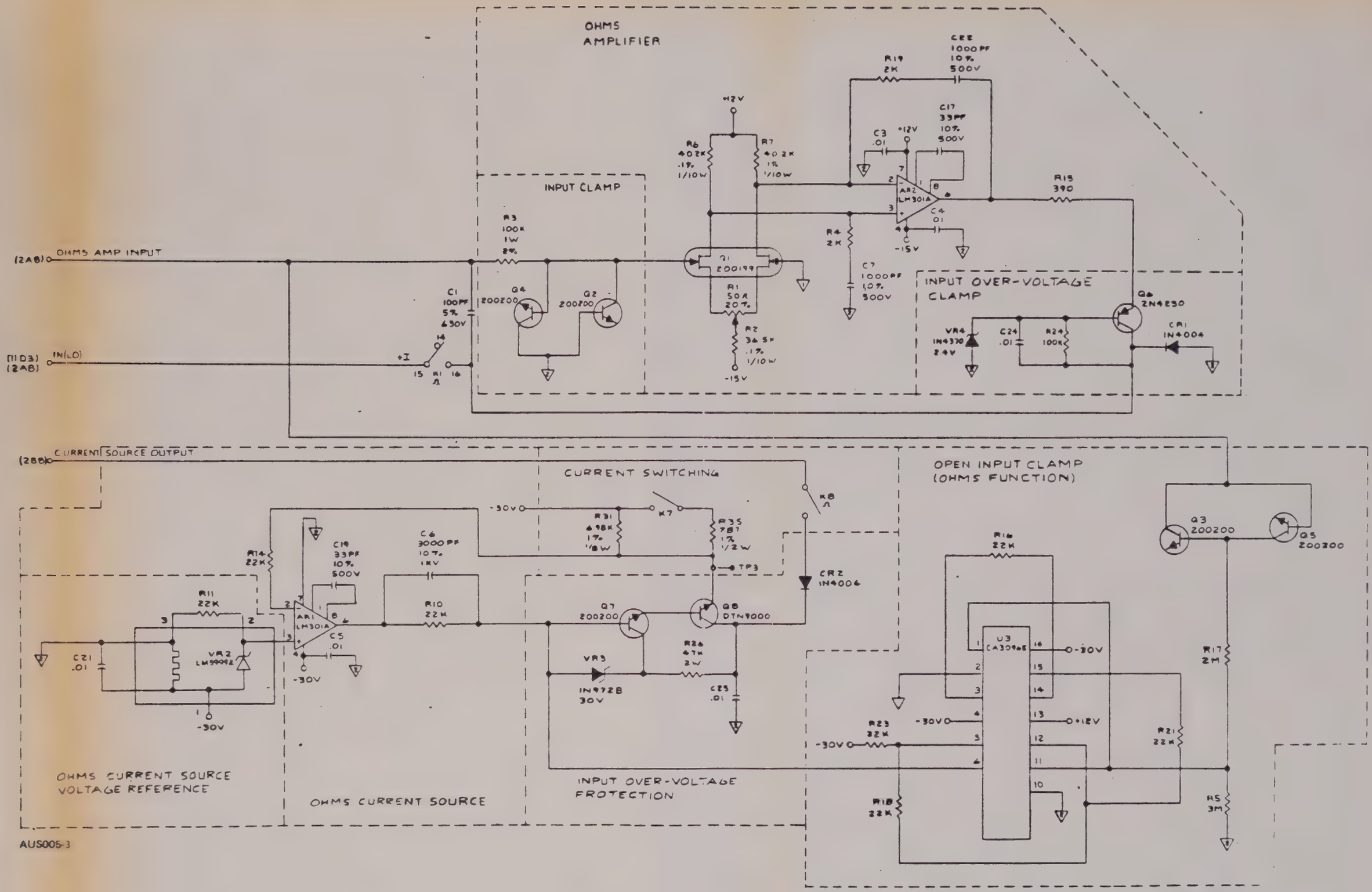


Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 3 of 11)

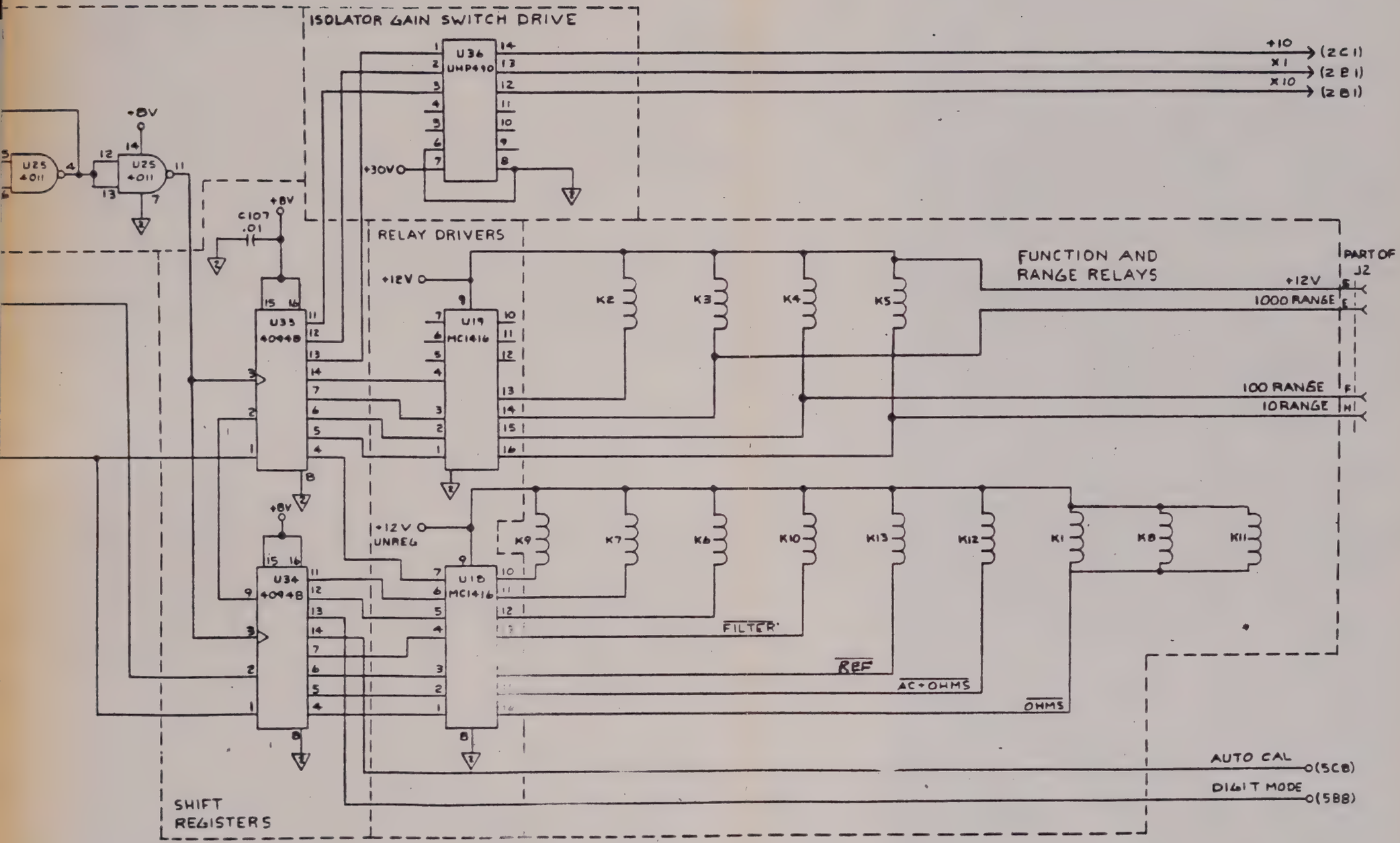
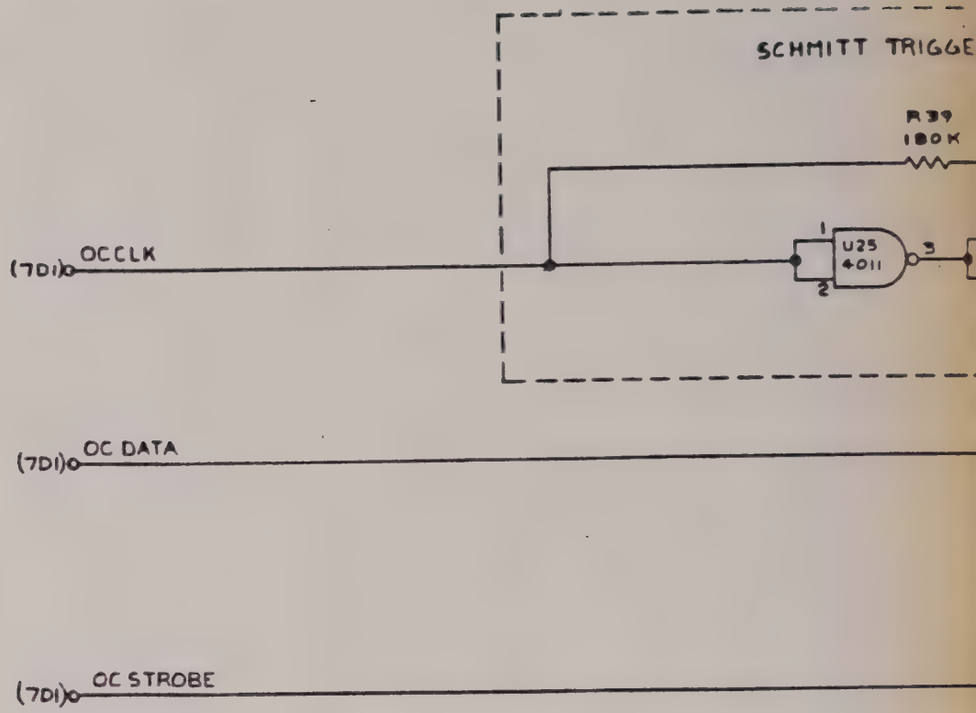


Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 4 of 11)



RANGE RELAY CHART

FUNCTION	RANGE	K2	K3	K4	K5	K6	K7	K9
DC	.1V							▨
	1V							▨
	10V							▨
	100V							
	1KV							
AC	1V							▨
	10V				▨			▨
	100V			▨				▨
	1KV		▨					▨
OHMS	.1KΩ					▨	▨	▨
	1KΩ					▨		▨
	10KΩ	▨		▨				▨
	100KΩ		▨	▨				▨
	1000KΩ			▨				▨
	10,000KΩ				▨			▨

▨ ENERGIZED

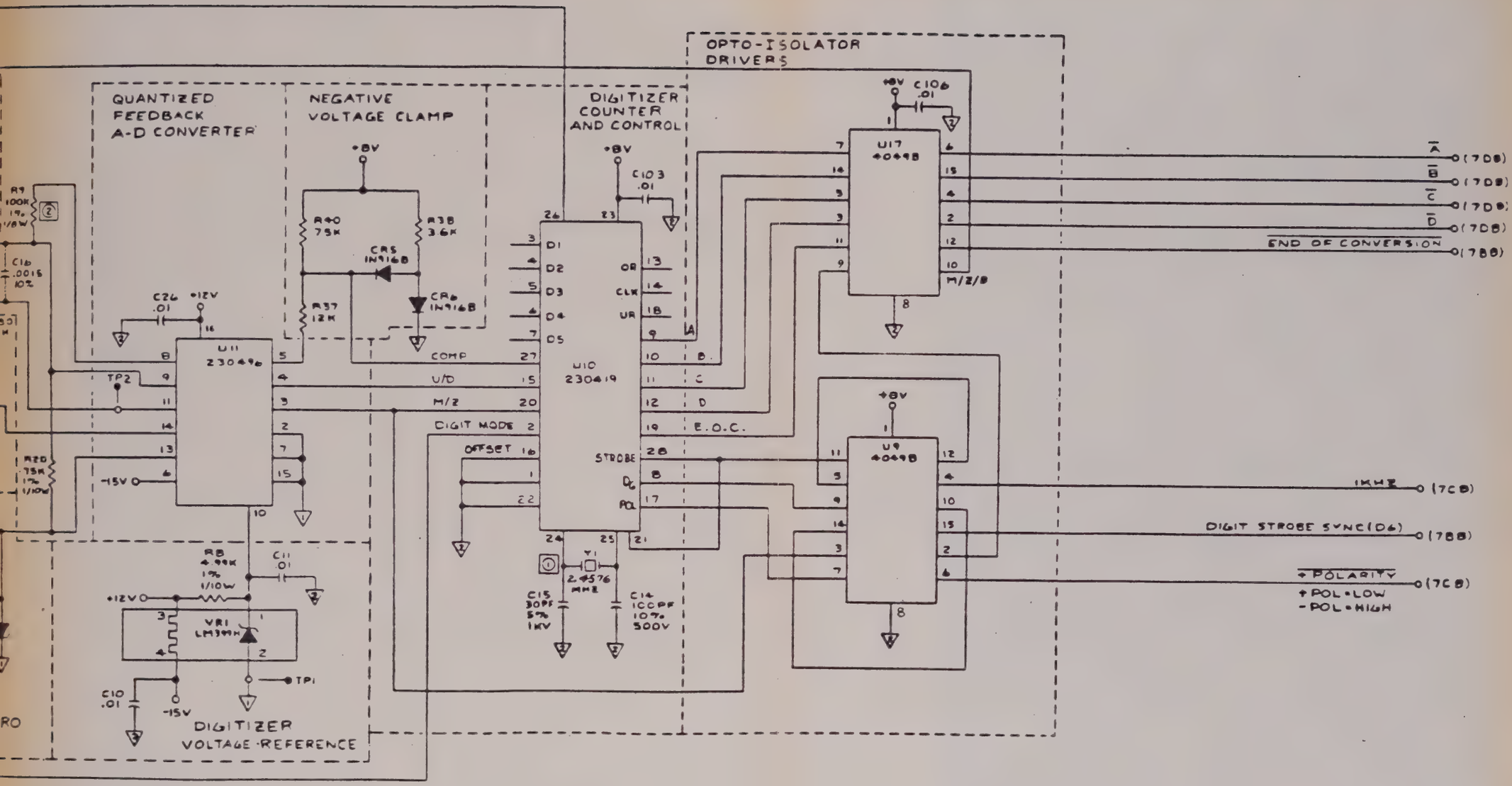
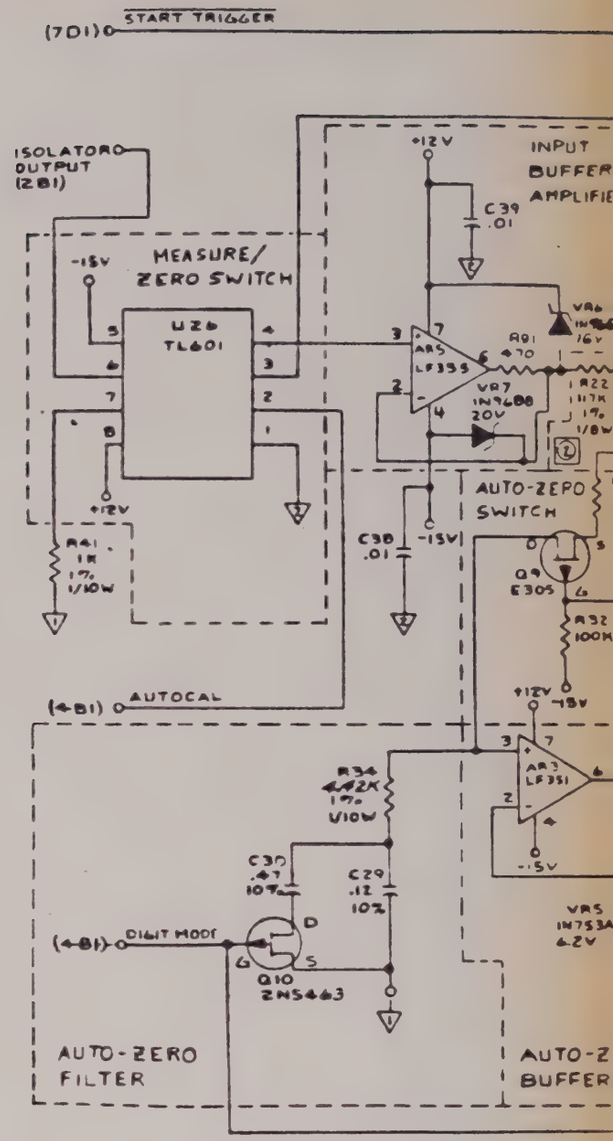


Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 5 of 11)



(2) R9 AND R22 IS MATCHED RESISTOR SET.

(1) 2.0576 MHZ FOR 60HZ
2.048 MHZ FOR 50HZ

NOTES: UNLESS OTHERWISE SPECIFIED THIS PAGE ONLY.

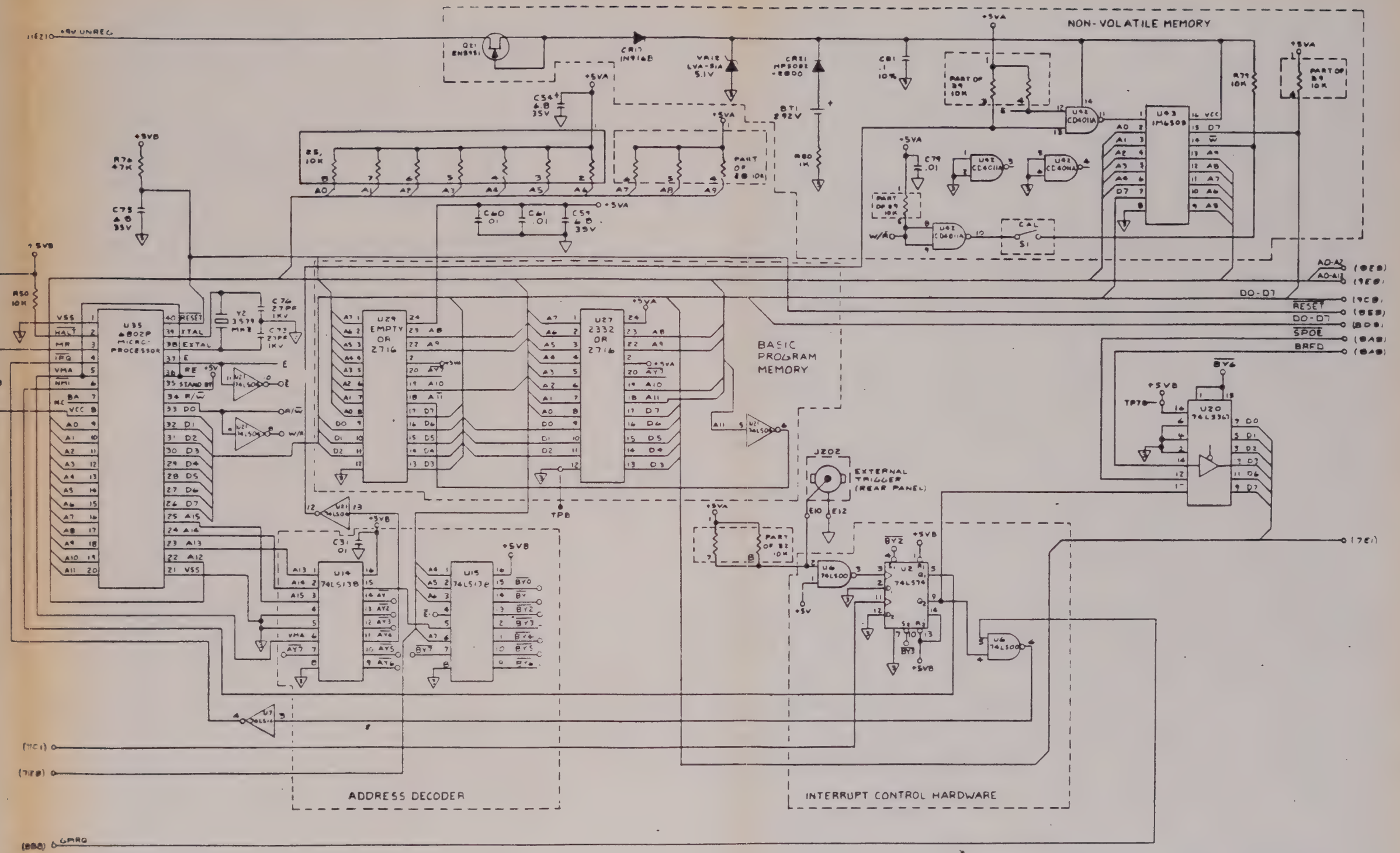
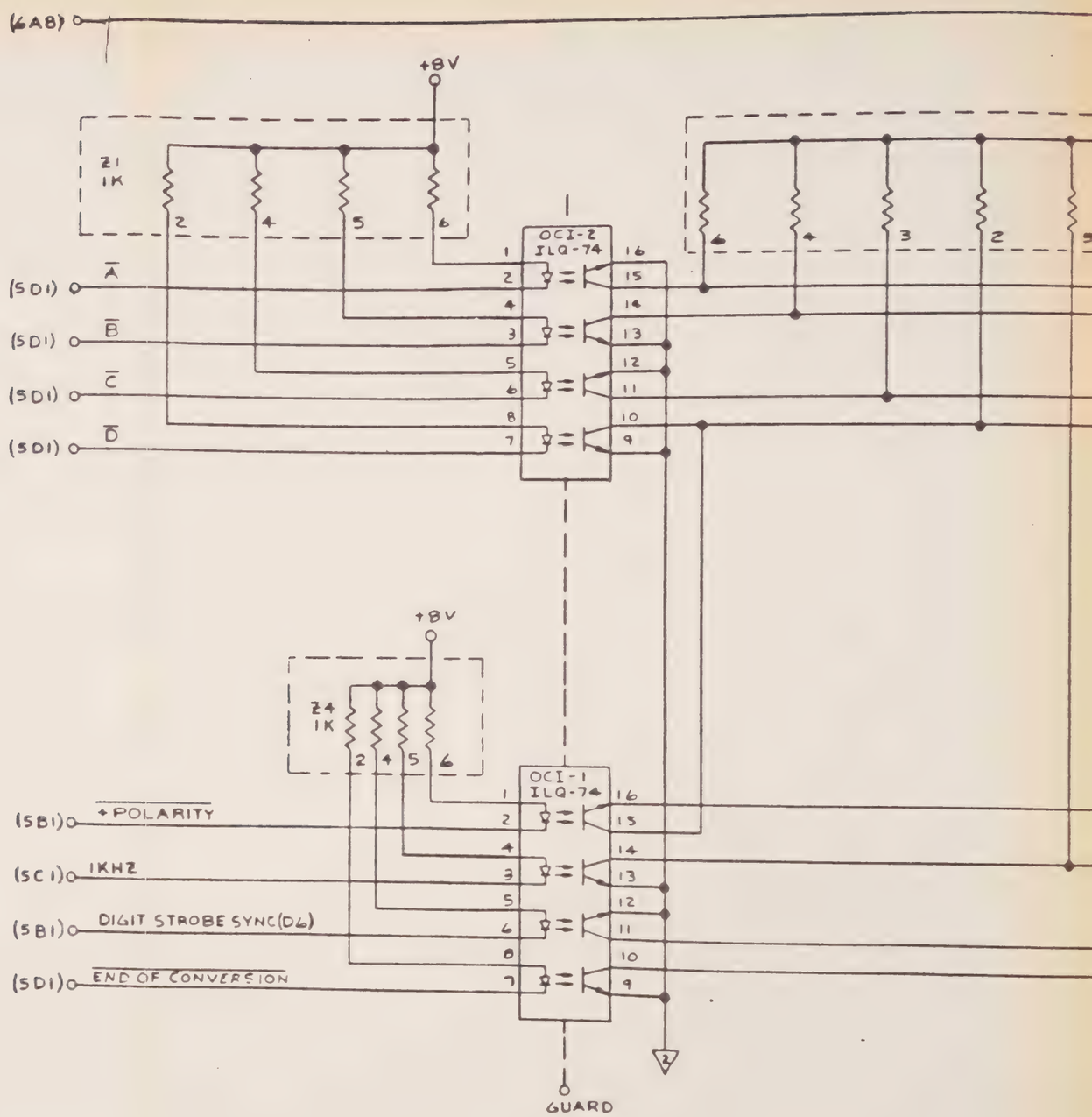


Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 6 of 11)

AUS005-6


(6AB)
+8V
Z1
1K
2
4
5
6
OCI-2
ILQ-74
1
2
4
3
5
6
8
7
16
15
14
13
12
11
10
9
(5DI) Ā
(5DI) B̄
(5DI) C̄
(5DI) D̄
+8V
Z4
1K
2
4
5
6
OCI-1
ILQ-74
(5BI) +POLARITY
(5CI) 1KHZ
(5BI) DIGIT STROBE SYNC(D6)
(5DI) END OF CONVERSION
GUARD

AUS005 7

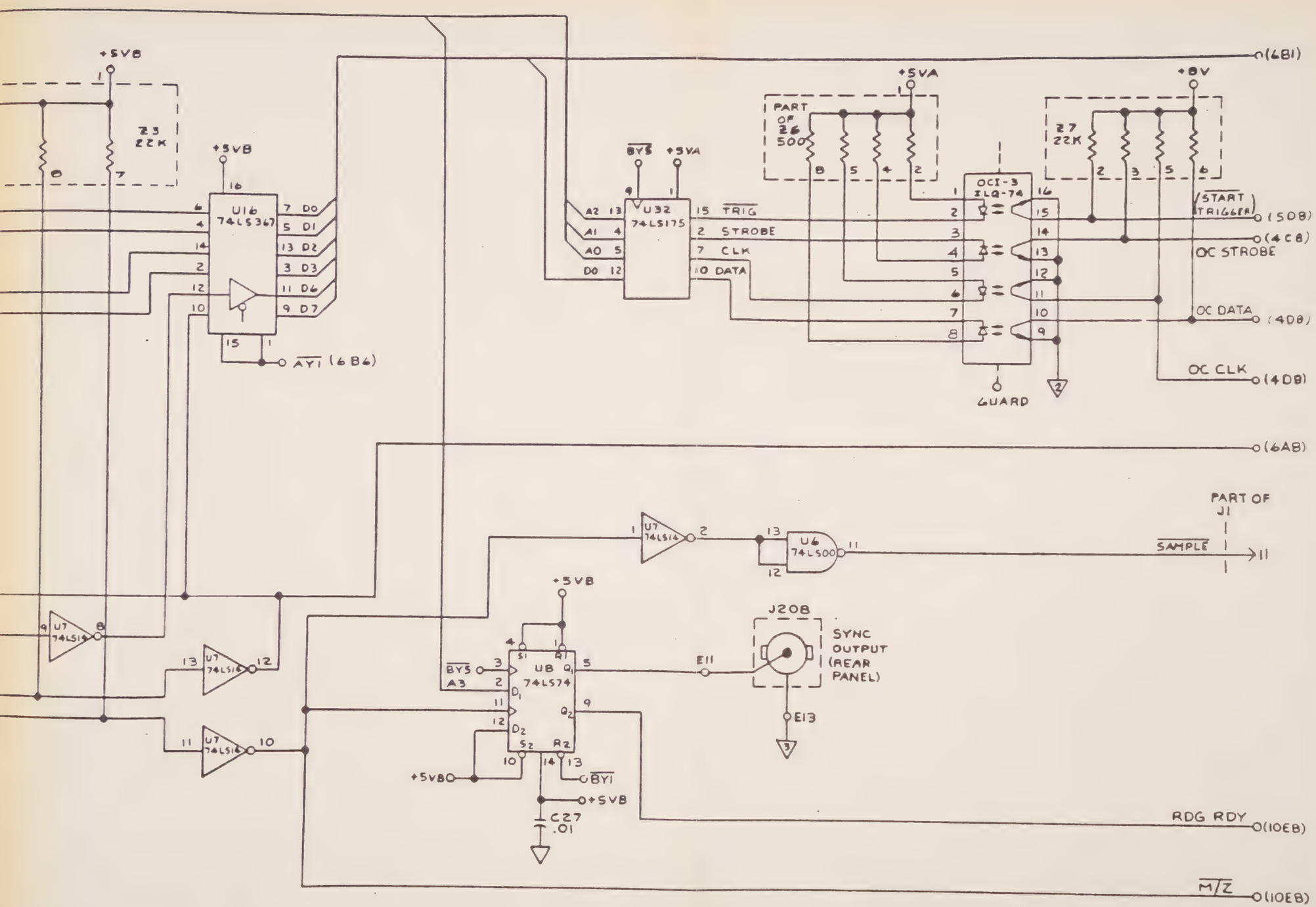
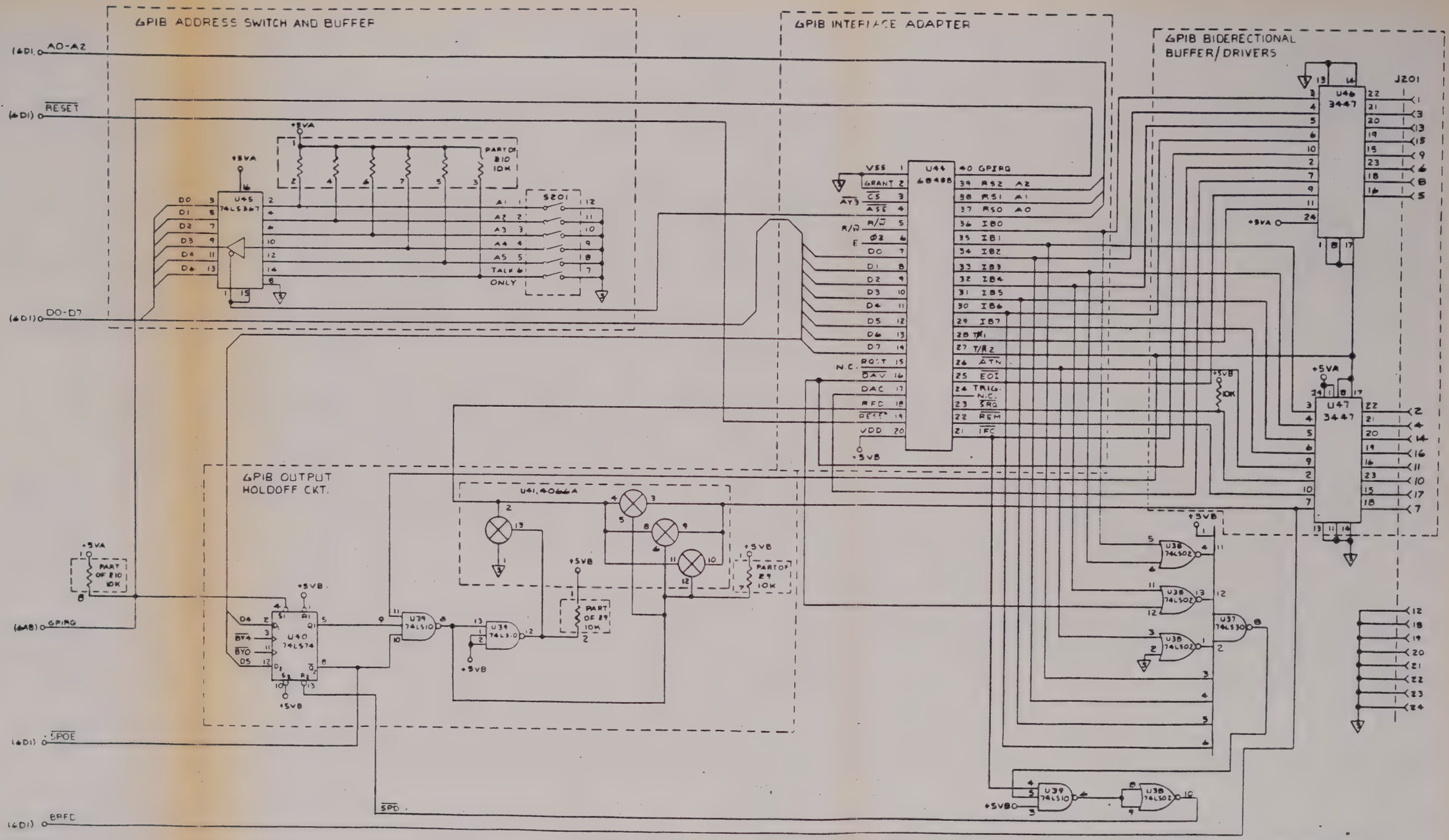


Figure 6-5. DMM Motherboard,
Schematic (431650 "A"
Sh. 7 of 11)



AUS005-8

Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 8 of 11)

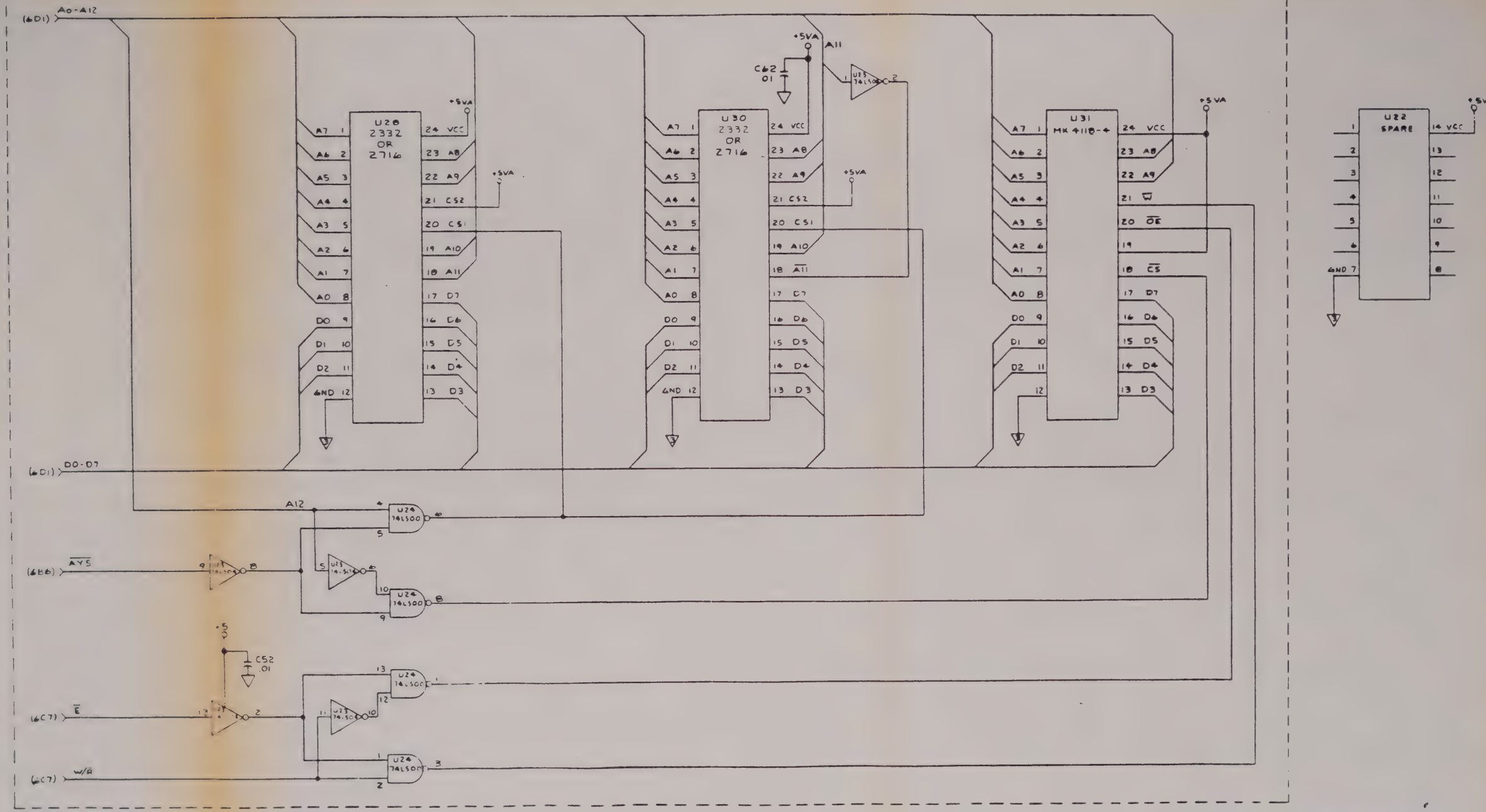


Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 9 of 11)

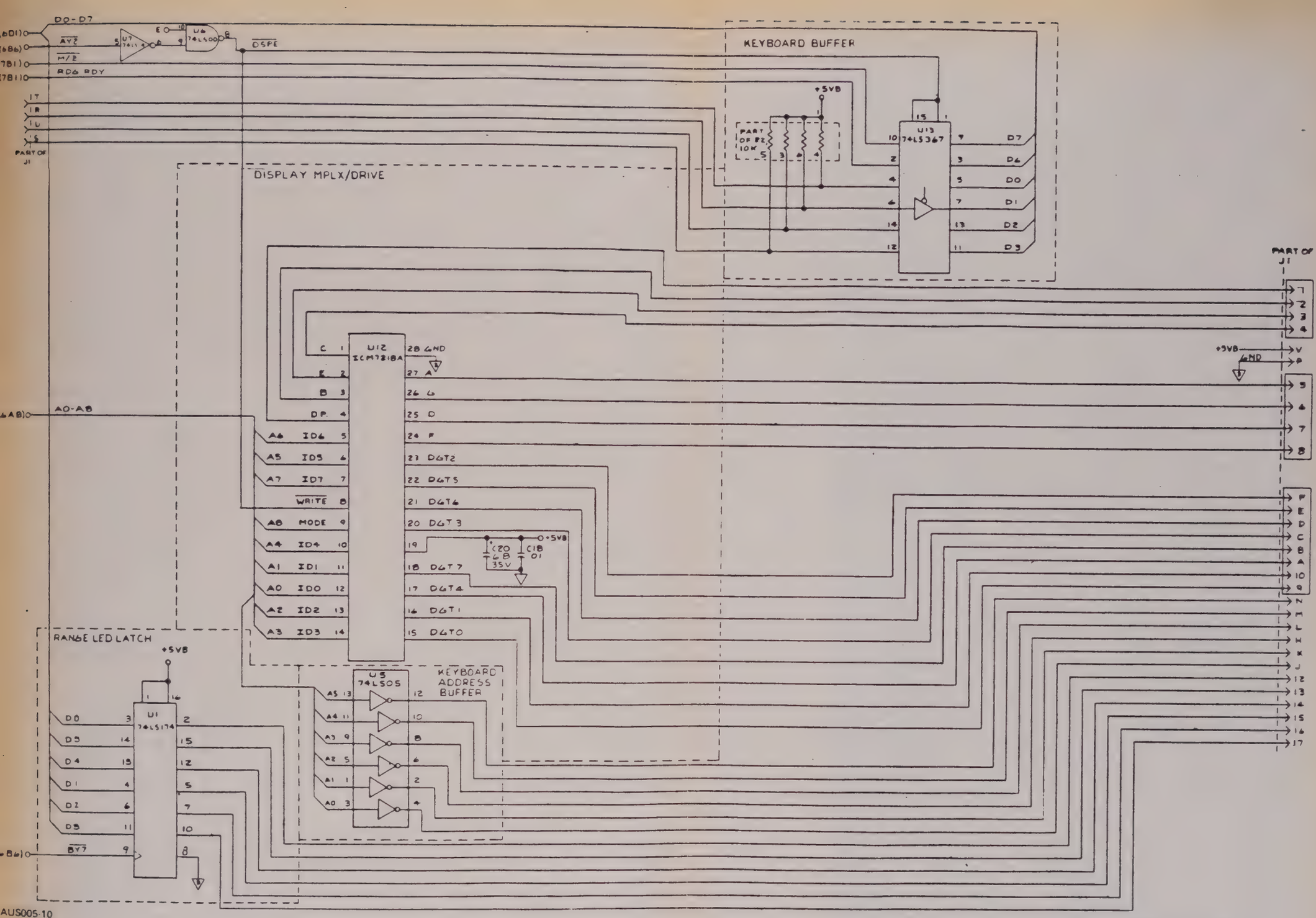
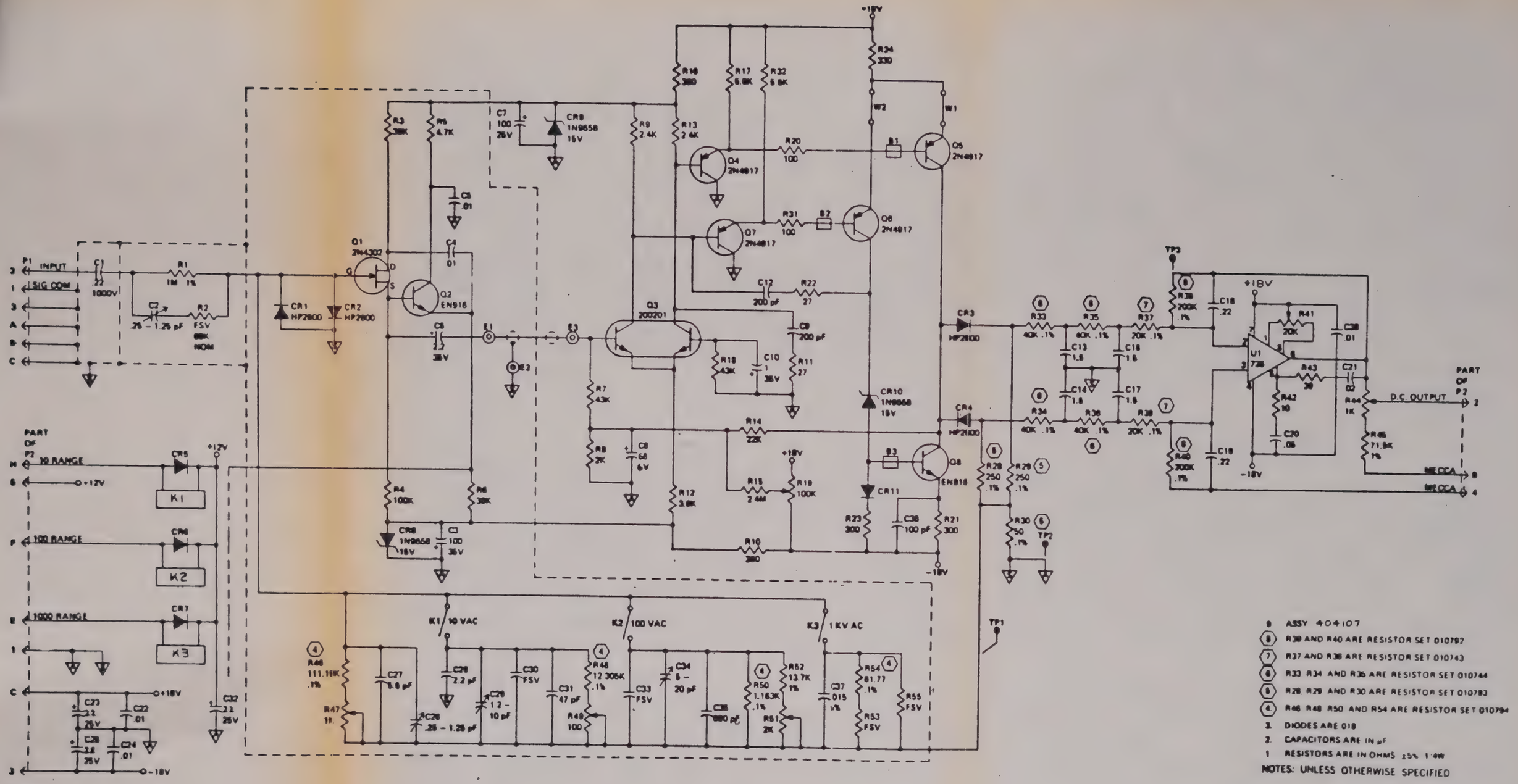


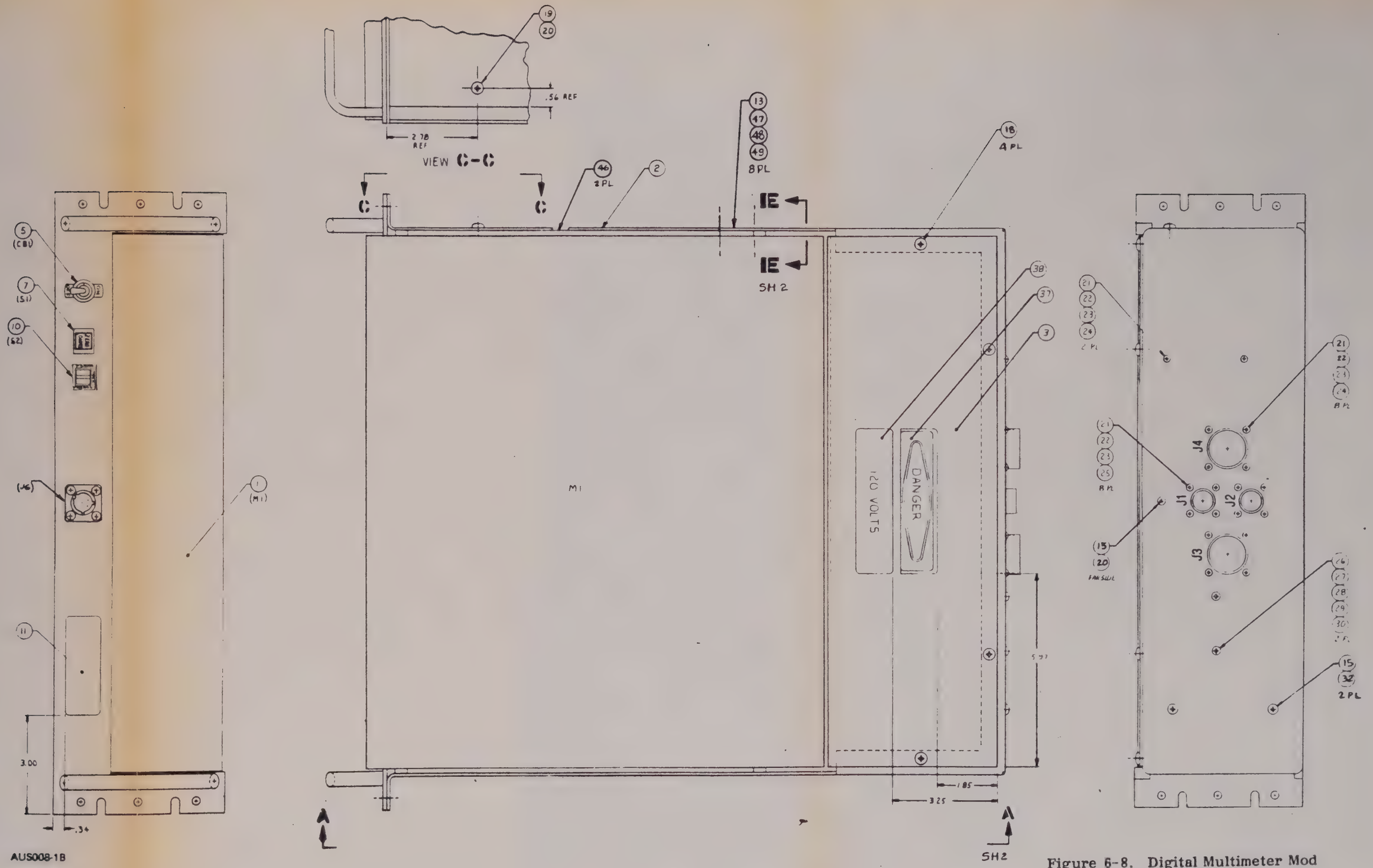
Figure 6-5. DMM Motherboard, Schematic (431650 "A" Sh. 10 of 11)



AUS007

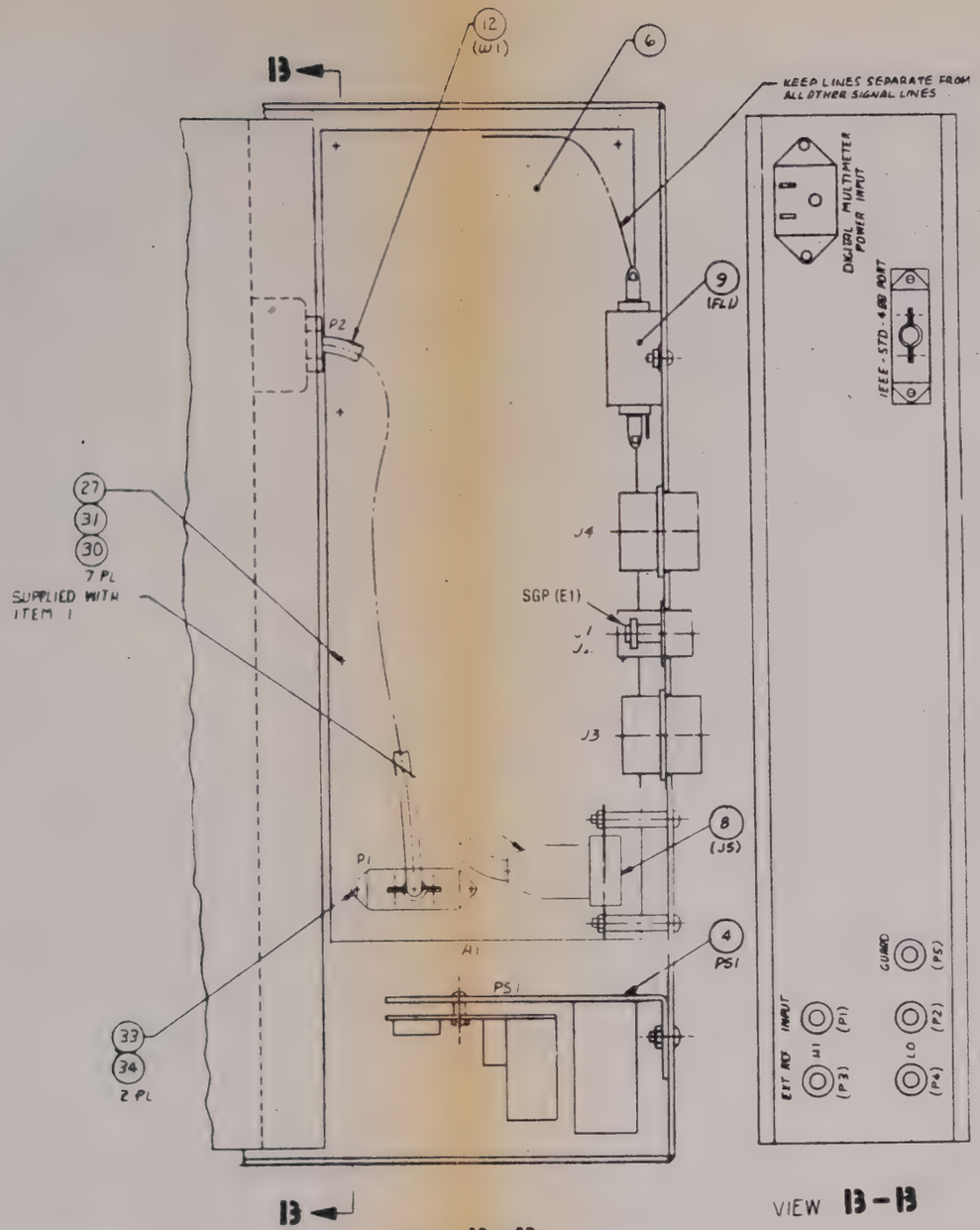
9 ASSY 404107
8 R30 AND R40 ARE RESISTOR SET 010792
7 R37 AND R39 ARE RESISTOR SET 010743
6 R33, R34 AND R35 ARE RESISTOR SET 010744
5 R28, R29 AND R30 ARE RESISTOR SET 010793
4 R46, R48, R50 AND R54 ARE RESISTOR SET 010794
3. DIODES ARE 018
2. CAPACITORS ARE IN pF
1 RESISTORS ARE IN OHMS ±5% 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

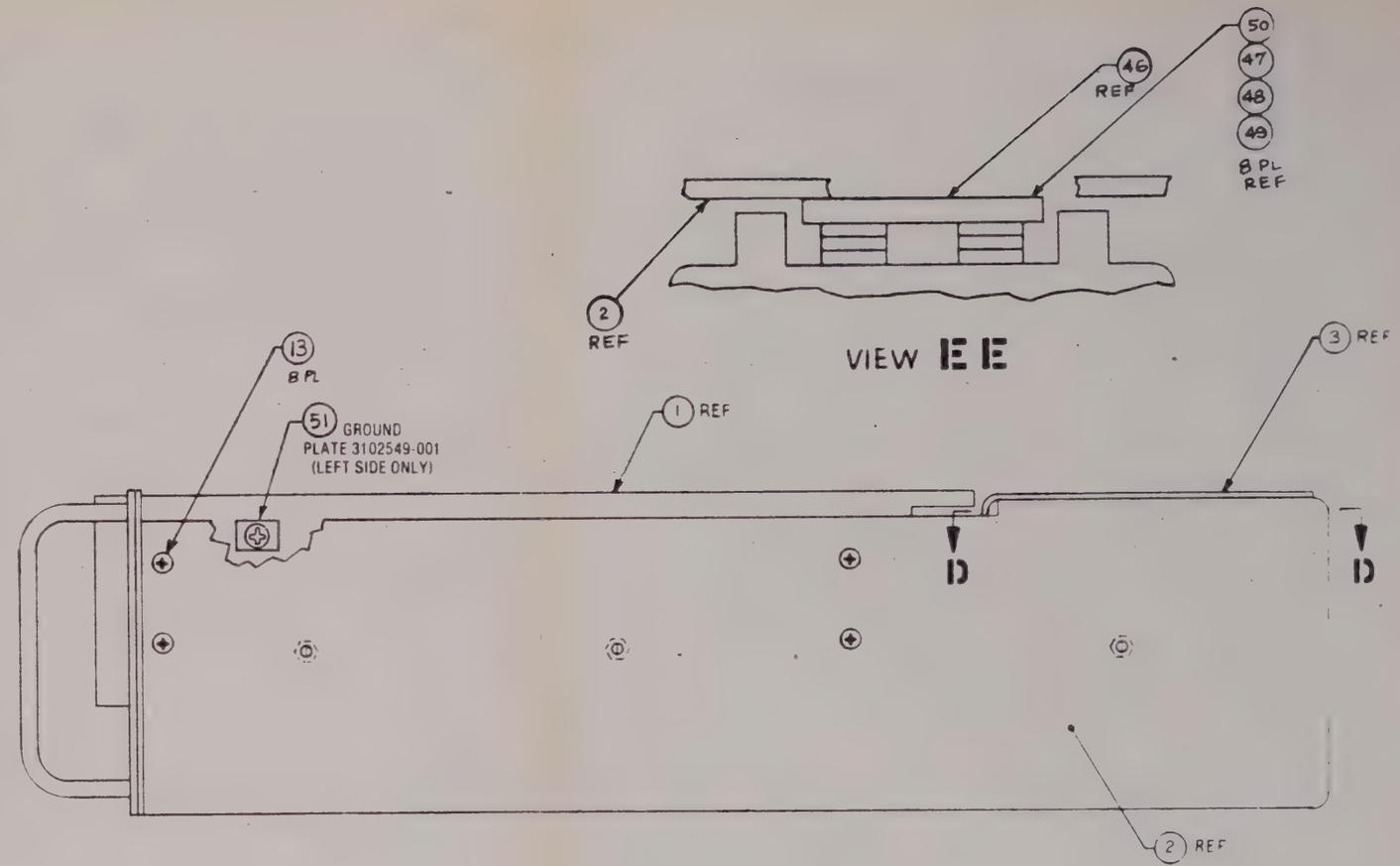
Figure 6-7.. DMM AC Converter Schematic (432131 "A")



AUS008-1B

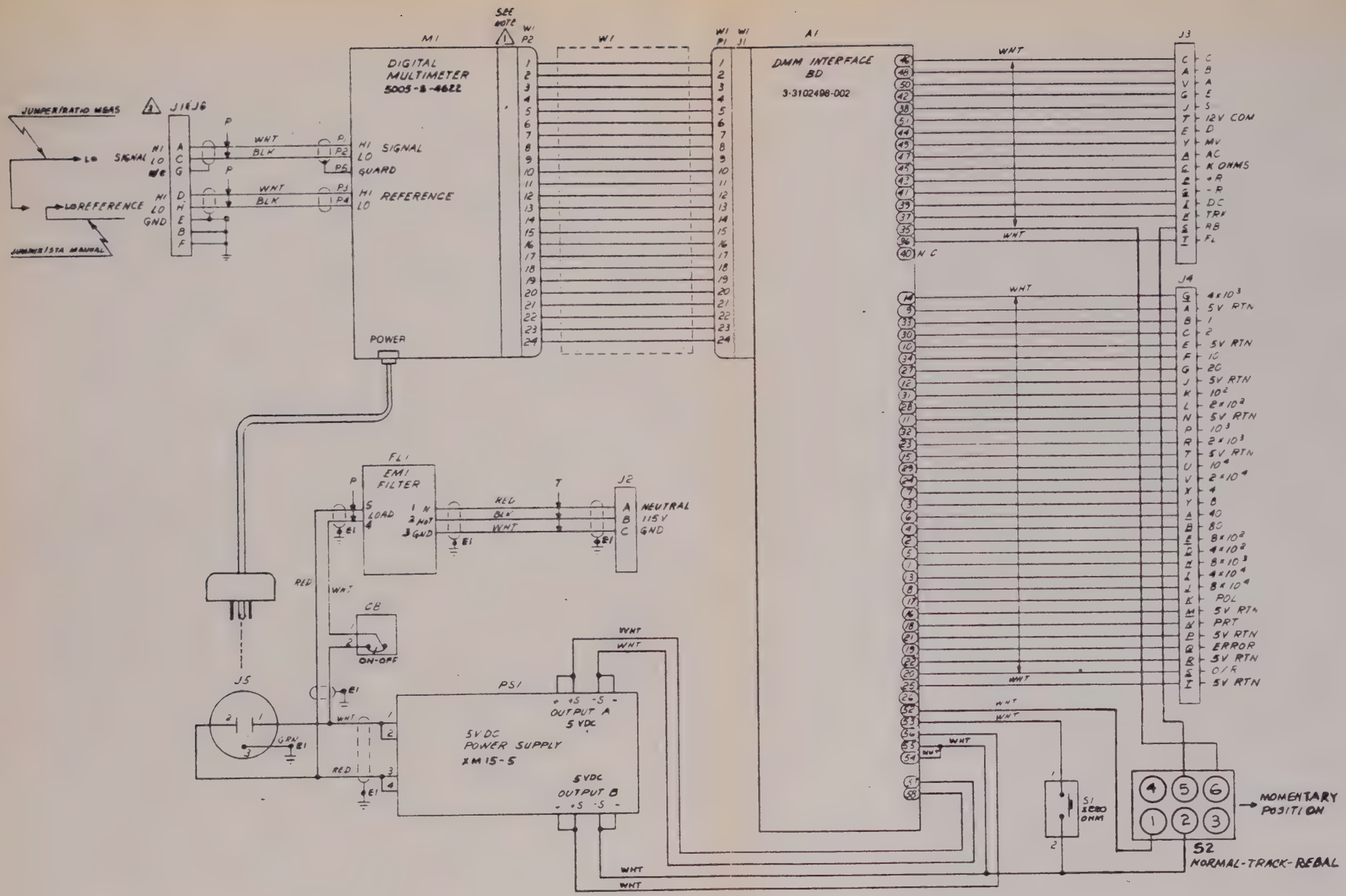
Figure 6-8. Digital Multimeter Mod Assembly (3102494) (Sh. 1 of 2)





AUS008-28

Figure 6-8. Digital Multimeter Mod Assembly (3102494) (Sh. 2 of 2)

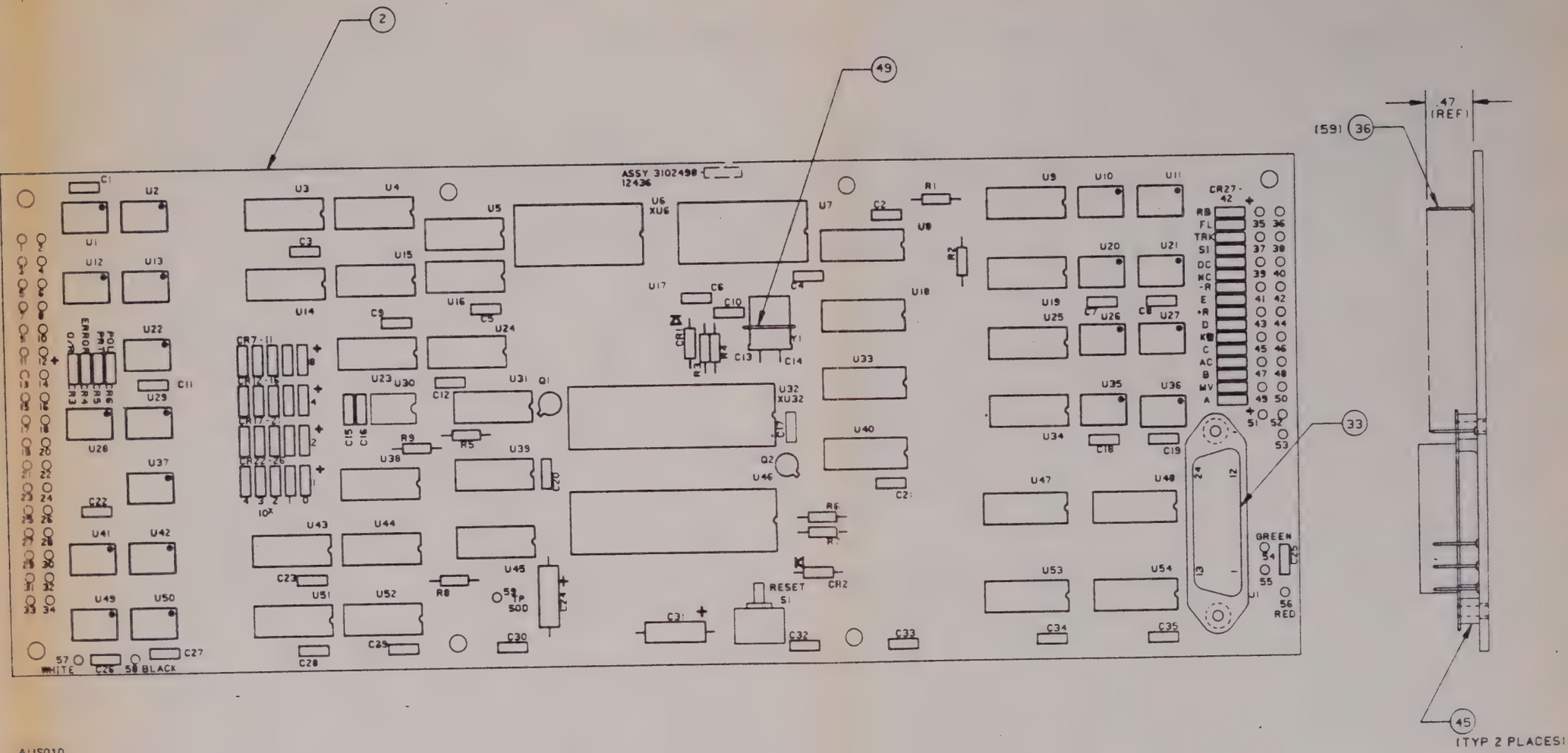


NOTE:

1. THIS CONNECTOR IS LABELED ON THE BACK OF THE DIGITAL MULTIMETER AS "IEEE-STD-488 PORT"
2. J1 AND J6 ARE CONNECTED IN PARRALLEL. J1 IS LOCATED AT THE REAR AND J6 AT THE FRONT OF THE INTERFACE CHASSIS.

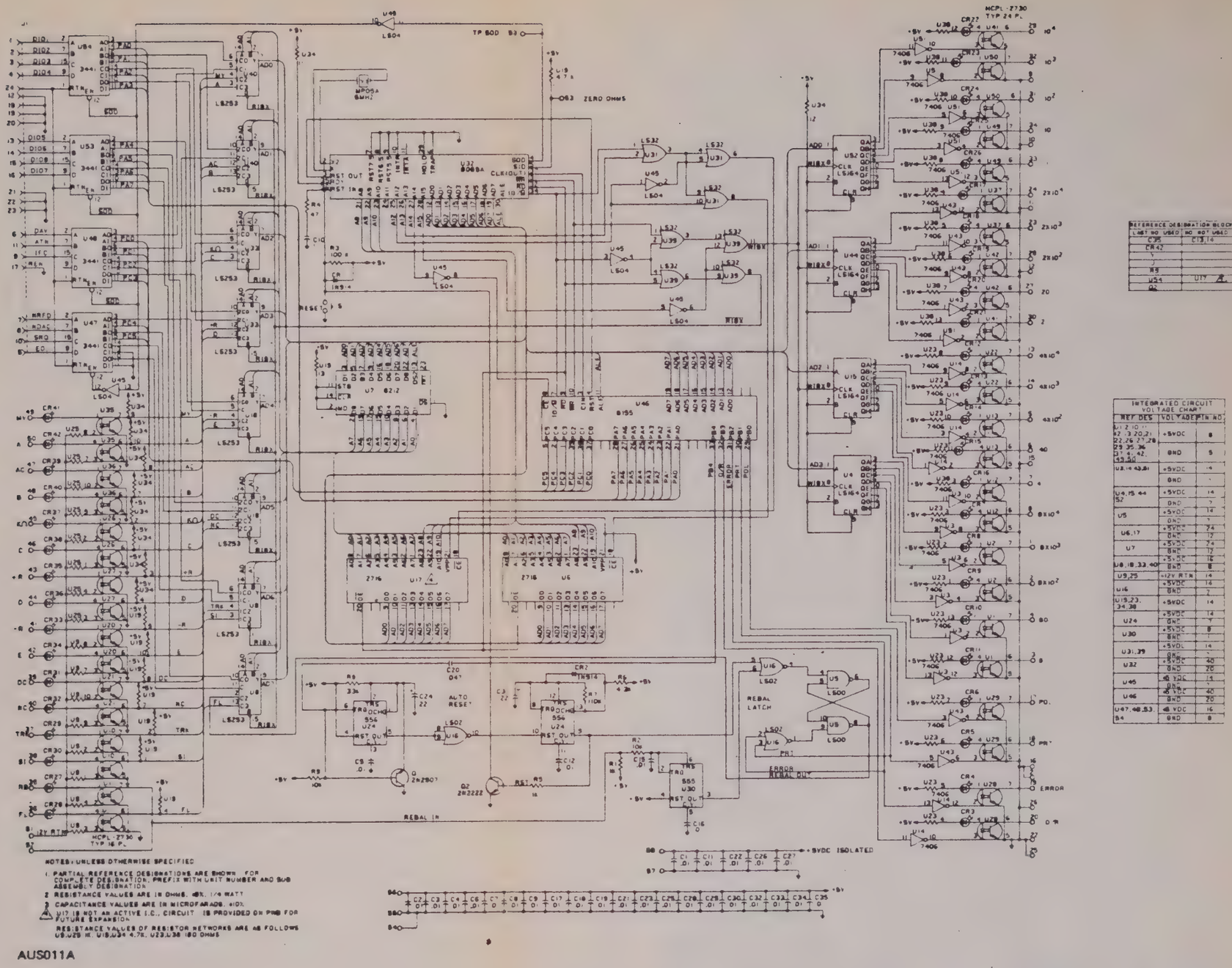
AUS009C

Figure 6-9. Digital Multimeter Mod Interconnection Diagram (3102570)



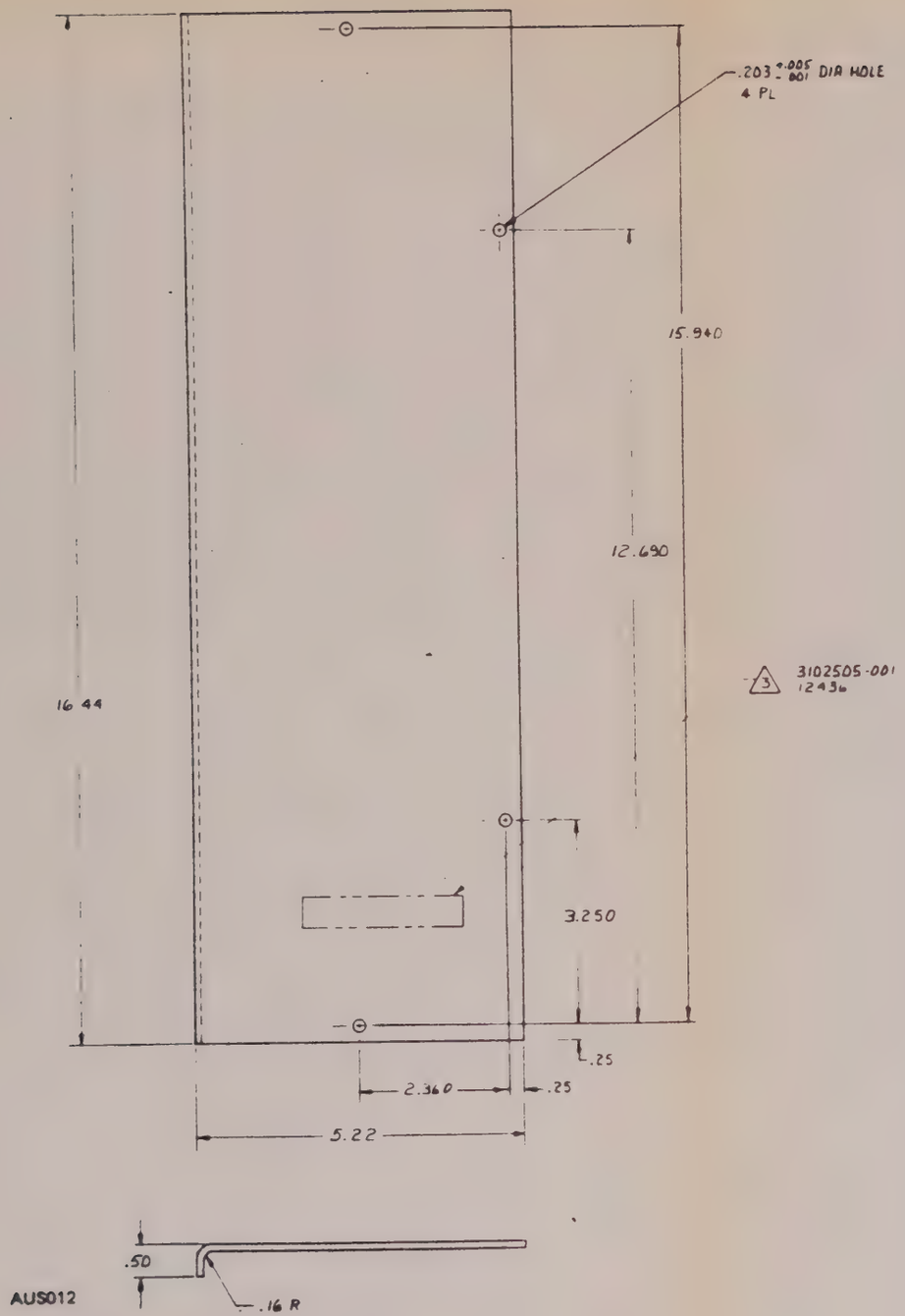
AUS010

Figure 6-10. Interface Circuit Card Assembly (3102498-003)



AUS011A

Figure 6-11. Interface Circuit Card Schematic Diagram (3102499)



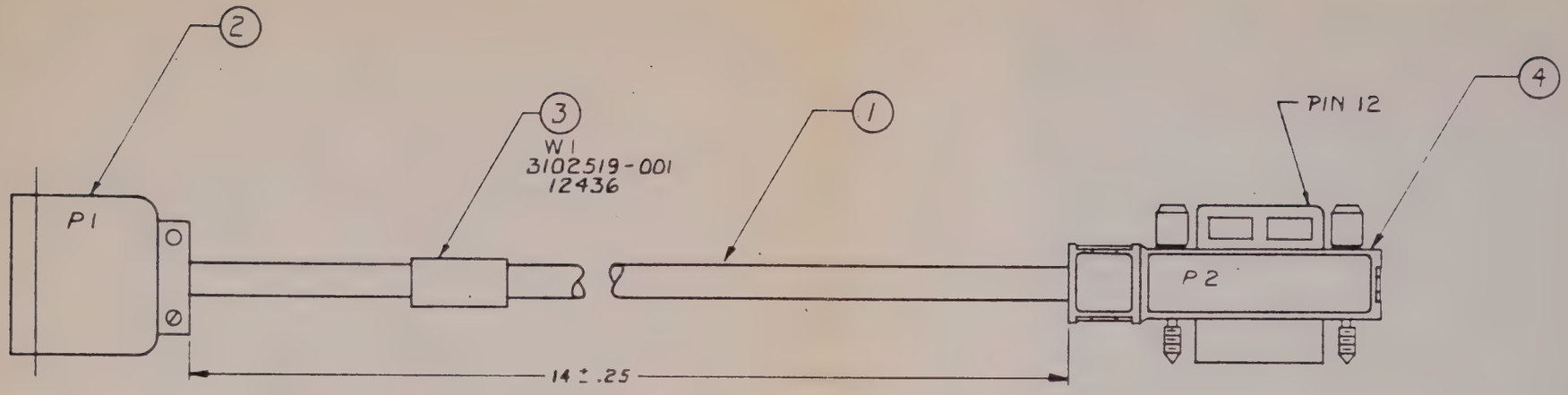
NOTES:

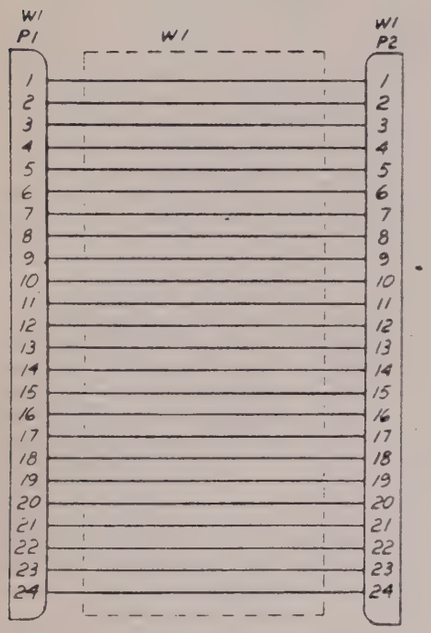
1 MATL: .090 THK 6061-T4 AL ALY PER QQ-A-250/11.

2 FINISH: CHEM FILM PER MIL-C-5541 CLASS 1A

3 MARK PART NO. FARSIDE APPROX AS SHOWN PER 3100123-001 TYPE I COLOR, BLACK

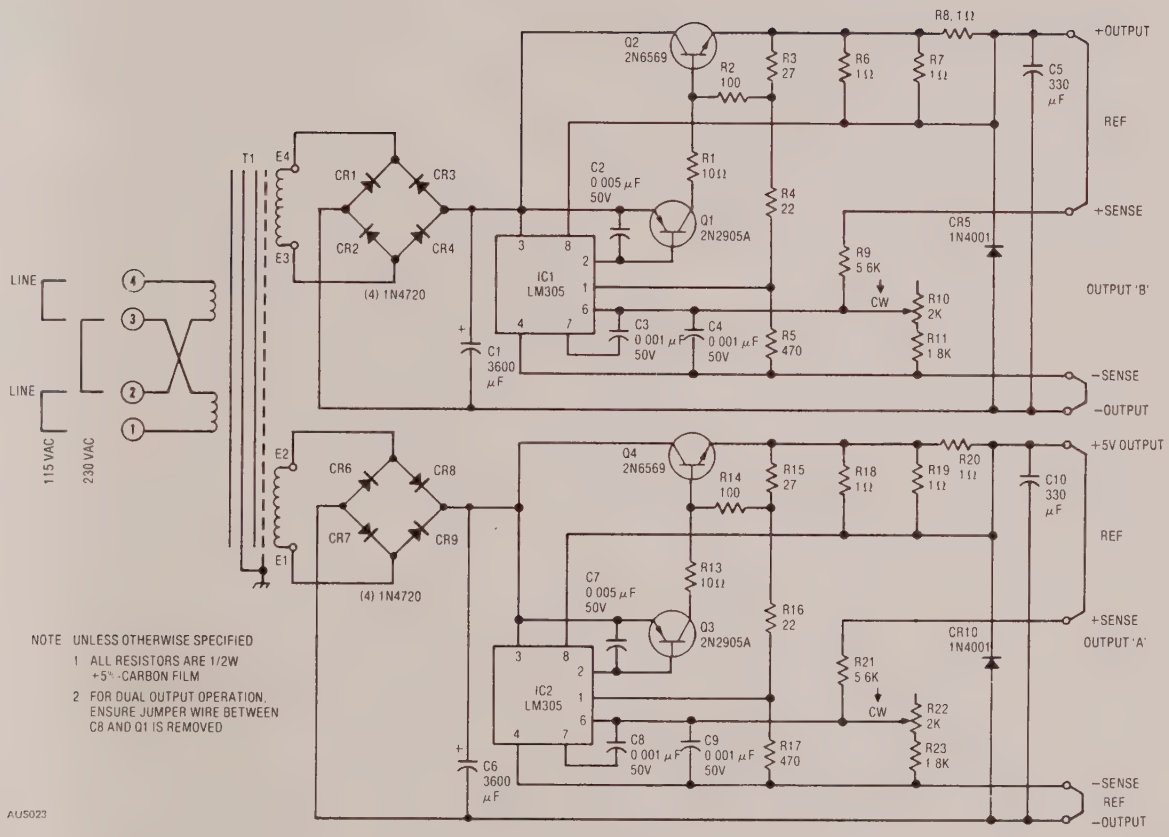
Figure 6-12. DMM Interface Cover (3102505)





AUS013

Figure 6-13. Interface Cable W1 Assembly (3102519)



PS1
MODEL XM-15-5

Figure 6-14. Interface Power Supply Schematic Diagram

SECTION 7

PARTS LIST

7-1. This section contains lists of replaceable parts for the assemblies in the order given in Table 7-1.

7-2. Manufacturers are identified by FSC numbers listed in Table 7-2. The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks, H4-1. H4-2, and their supplements.

Table 7-1. List of Drawings

DWG. NO.	TITLE	FIGURE NO.	TABLE
404104	DMM Chassis Assembly	6-1	7-3
401651	DMM Display, PCB Assembly	6-2	7-4
401650	DMM Motherboard, PCB Assembly	6-4	7-5
404107	DMM AC Converter, PCB Assembly	6-6	7-6
3102494	Digital Multimeter Mod Assembly	6-8	7-7
3102498	Interface Circuit Card Assembly	6-10	7-8
3102519	Interface Cable W1 Assembly	6-13	7-9

Table 7-2. List of Suppliers

FSC	NAME
00779	AMP, INC. HARRISBURG, PENNSYLVANIA
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN
01281	TRW SEMICONDUCTORS LAWNDALE, CALIFORNIA
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
02114	FERROXCUBE CORP. SAUGERTIES, NEW YORK
02660	AMPHENOL CORP. BROADVIEW, ILLINOIS
02668	GUY P. HARVEY & SON CORP. LEOMINSTER, MAINE
02735	RCA SOLID STATE DIV. SOMERVILLE, NEW JERSEY
03888	PYROFILM CORP. WHIPPANY, NEW JERSEY
04222	AEROVOX CORP. (HI-Q DIV.) MYRTLE BEACH, SOUTH CAROLINA
04713	MOTOROLA, INC. (SEMI-CONDUCTOR PRODUCTS DIV.) PHOENIX, ARIZONA
05245	CORCAM INC. LIBERTYVILLE, ILLINOIS
05276	POMONA ELECTRONICS CO., INC. POMONA, CALIFORNIA
05397	UNION CARBIDE CORP. (MATERIALS SYSTEMS DIV.) CLEVELAND, OHIO
06665	PRECISION MONOLITHICS SANTA CLARA, CALIFORNIA
07263	FAIRCHILD (SEMICONDUCTOR DIV.) MOUNTAIN VIEW, CALIFORNIA
07716	TRW ELECTRONIC COMPONENTS (IRC) BURLINGTON, IOWA
08257	NPC ELECTRONICS CANOGA PARK, CALIFORNIA
09023	CORNELL-DUBILIER ELECTRONICS SANFORD, NORTH CAROLINA
11236	CTS OF BERNE, INC. BERNE, INDIANA
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
12436	GENERAL DYNAMICS CORP. ELECTRONICS DIV. SAN DIEGO, CALIFORNIA
15636	ELEC-TROL, INC. SAUGUS, CALIFORNIA
16438	BELDEN CORP. ELECTRONIC DIV. RICHMOND, INDIANA
19048	REPLACED BY 02660
21317	ELECTRONIC APPLICATIONS CO. SO. EL MONTE, CALIFORNIA
21551	C-F ELECTRONICS, INC. VAN NUYS, CALIFORNIA
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CALIFORNIA
23223	CTS MICROELECTRONICS INC. LAFAYETTE, ILLINOIS
24355	ANALOG DEVICES NORWOOD, MASSACHUSETTS
26625	MIAL USA, INC. NUTLEY, NEW JERSEY

FSC	NAME
26806	AMERICAN ZETTLER, INC. COSTA MESA, CALIFORNIA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
27777	VARO ELECTRAN DEVICES, INC. GARLAND, TEXAS
32293	INTERSIL, INC. CUPERTINO, CALIFORNIA
34553	AMPEREX/MEPCO-ELECTRA (COMPONENT DIV.) HAUPPAUGE, NEW YORK
34649	INTEL CORP. ALOHA, OREGON
50088	MOSTEK CORP. CARROLLTON, TEXAS
50434	HEWLETT-PACKARD CO. (HPA DIV.) PALO ALTO, CALIFORNIA
50579	LITRONIX, INC. CUPERTINO, CALIFORNIA
50857	DIONICS, INC WESTBURY, NEW YORK
52763	STETTNER-TRUSH CAZENOVIA, NEW YORK
53279	XEMTEX INC. SAN MARCOS, CALIFORNIA
56289	SPRAGUE ELECTRIC CO. N. ADAMS, MASSACHUSETTS
58189	REPLACED BY 12436
59730	THOMAS & BETTS CORP. IOWA CITY, IOWA
71279	CAMBRIDGE THERMIONIC CORP. CAMBRIDGE, MASSACHUSETTS
71471	AEROVOX CORP. (CINEMA PLANT) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS MILWAUKEE, WISCONSIN
71707	COTO-COIL CO., INC. PROVIDENCE, RHODE ISLAND
71785	TRW ELECTRONIC COMPONENTS (CINCH DIV.) ELK GROVE VILLAGE, ILLINOIS
72619	DIALIGHT DIV. AMPEREX ELECTRONIC CORP. BROOKLYN, NEW YORK
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, L.I., NEW YORK
74970	E. F. JOHNSON CO. WASECA, MINNESOTA
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
80205	NAS STANDARD
81073	GRAYHILL INC. LA GRANGE, ILLINOIS
81349	MILITARY SPECIFICATION
81350	SEE 81349
81541	AIRPAX ELECTRONICS INC. CAMBRIDGE, MARYLAND

FSC	NAME
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
88044	AERONAUTICAL STANDARDS GROUP DEPARTMENT OF NAVY & AIR FORCE
90201	MALLORY CAPACITOR CO. INDIANAPOLIS, INDIANA
91637	DALE ELECTRONICS, INC. COLUMBUS, NEBRASKA
96906	MIL STANDARD

Table 7-3. DMM Chassis Assembly 404104

REF DES	DESCRIPTION	FSC	MANU P/N
F201	FUSE SLO .50A 250V	75915	3AG1/2ASB
J101	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J102	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J103	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J104	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J105	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J201	RECEPT 24 POS	00779	552791-1
J202	CONN BNC	02660	31-010
J203	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J204	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J205	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J206	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J207	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J208	CONN BNC	02660	31-010
J209	CONN RECPTLE	82389	EAC-301
S201	SWITCH 6 SPST	11237	206-6

Table 7-4. DMM Display, PCB Assembly 4016541

REF DES	DESCRIPTION	FSC	MANU P/N
CR1	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR2	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR3	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR4	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR5	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR6	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR7	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR8	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR9	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR10	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR11	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR12	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR13	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR14	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR15	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR16	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR17	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR18	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR19	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR20	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR21	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR22	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
DS1	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS2	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS3	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS4	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS5	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS6	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS7	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
P1	CONN 18 P	71785	252-18-30-160
R1	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R2	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R3	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R4	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R5	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R6	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R7	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R8	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
U1	IC DRIVER UDN-2981A	56289	UDN-2981A
U2	IC	01295	SN7417
U3	IC	01295	SN7417
Z1	RES CERMET 6.8 K Network 16P,8R 2%	11236	761-3-R6.8K
Z2	RES CERMET 200 OHM Network 8P,7R 2%	11236	750-81-R220

Table 7-5. DMM Motherboard, PCB Assembly 401650

REF DES	DESCRIPTION	FSC	MANU P/N
AR1	IC OP AMP	27014	LM301A
AR2	IC OP AMP	27014	LM301A
AR3	IC OP AMP LF351N	27014	LF351N
AR5	IC	27014	LF355H
AR6	IC OP AMP	27014	LM301A
AR7	IC HI VOLTAGE OP AMP	27014	LM343H
AR8	IC OP AMP LF351N	27014	LF351N
AR9	IC OP AMP AD517KH	24355	AD517KH
BT1	BATTERY 3 VOLT LITHIUM ORGANIC	90201	L032S
C1	CAP POLY 100 PFD 630 V 5%	08257	KSO Series
C3	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C4	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C5	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C6	CAP CERAM .003 PFD 1000 V 10%	71590	DD302
C7	CAP CERAM .001 MFD 500 V 10%	04222	SCD-DI-2X5F-1000
C10	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C11	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C14	CAP CERAM 100 PFD 500 V 10%	04222	TCD-DI-1N5600-100
C15	CAP CERAM 30 PFD 1000 V 5%	56289	C030B102F300J
C16	CAP MYLAR .0015 MFD 100 V 10%	09023	WMF1S47
C17	CAP CERAM 33 PFD 500 V 10%	71471	TCD-DI-1(N750)
C18	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C19	CAP CERAM 33 PFD 500 V 10%	71471	TCD-DI-1(N750)
C20	CAP TANTA 6.8 MFD 35 V 20%	05397	T368B685M035AS
C21	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C22	CAP CERAM .001 MFD 500 V 10%	04222	SCD-DI-2X5F-1000
C24	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C25	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C26	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C27	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C29	CAP MYLAR .12 F 100 V 10%	09023	WMF1P12
C30	CAP MYLAR .47 MFD 100 V 10%	27556	SAZB474K
C31	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C38	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C39	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C45	CAP POLY .15 F 50 V 10%	09023	MCR1P15
C46	CAP CERAM 200 PFD 1000 V 20%	56289	C023B102E201M
C47	CAP CERAM 47 PFD 500 V 10%	71471	TCD-DI-2(N750)
C49	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C50	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C52	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C53	CAP POLY .001 MFD 500 V 5%	08257	KSO Series
C54	CAP TANTA 6.8 MFD 35 V 20%	05397	T368B685M035AS
C55	CAP POLY .15 F 50 V 10%	09023	MCR1P15
C56	CAP CERAM 33 PFD 500 V 10%	71471	TCD-DI-I(N750)
C58	CAP POLY .15 F 50 V 10%	09023	MCR1P15
C59	CAP TANTA 6.8 MFD 35 V 20%	05397	T368B685M035AS

Table 7-5. DMM Motherboard, PCB Assembly 401650 (Continued)

REF DES	DESCRIPTION						FSC	MANU P/N
C60	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C61	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C62	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C63	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C64	CAP	CERAM	.003	PFD	1000 V	10%	71590	DD302
C65	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C66	CAP	ELECT	10,000	F	16 V			VP16VB10000MC
C67	CAP	CERAM	.1	MFD	100 V	20%	72982	845-000-X5V01042
C68	CAP	CERAM	.1	MFD	100 V	20%	72982	845-000-X5V01042
C69	CAP	CERAM	.001	MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C70	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C71	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C72	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C73	CAP	CERAM	27	PFD	1000 V	10%	71590	DD270
C74	CAP	CERAM	.003	PFD	1000 V	10%	71590	DD302
C75	CAP	TANTA	6.8	MFD	35 V	20%	05397	T368B685M035AS
C76	CAP	CERAM	27	PFD	1000 V	10%	71590	DD270
C77	CAP	ELECT	1000	MFD	35 V			35TAL1000
C79	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C80	CAP	ELECT	1000	MFD	35 V			35TAL1000
C81	CAP	MYLAR	.1	MFD	100 V		09023	WMF1P1
C82	CAP	ELECT	4700	MFD	16 V			16TAL4700
C84	CAP	ELECT	470	MFD	50 V	Radial Lead		See Description
C85	CAP	ELECT	470	MFD	50 V	Radial Lead		See Description
C88	CAP	TANTA	6.8	MFD	35 V	20%	05397	T368B685M035AS
C89	CAP	TANTA	6.8	MFD	35 V	20%	05397	T368B685M035AS
C90	CAP	TANTA	10	MFD	50 V	10%	05397	T362C106K050A
C95	CAP	TANTA	6.8	MFD	35 V	20%	05397	T368B685M035AS
C96	CAP	TANTA	6.8	MFD	35 V	20%	05397	T368B685M035AS
C97	CAP	TANTA	10	MFD	50 V	10%	05397	T362C106K050A
C98	CAP	TANTA	6.8	MFD	35 V	20%	05397	T368B685M035AS
C99	CAP	CERAM	.01	MFD	2000 V		71471	HVD6-2KV
C100	CAP	CERAM	.01	MFD	2000 V		71471	HVD6-2KV
C101	CAP	TANTA	2.2	MFD	35 V	20%	05397	T368B225M035AS
C102	CAP	TANTA	2.2	MFD	35 V	20%	05397	T368B225M035AS
C103	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C106	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
C107	CAP	CERAM	.01	MFD	100 V	20%	56289	C023B101F103M
CR1	DIODE	SILICO					81349	1N4004
CR2	DIODE	SILICO					81349	1N4004
CR5	DIODE	SILICO			1N916B		81349	1N916B
CR6	DIODE	SILICO			1N916B		81349	1N916B
CR9	DIODE	SILICO			1N916B		81349	1N916B
CR10	DIODE	SILICO			1N916B		81349	1N916B
CR11	DIODE	SILICO			1N916B		81349	1N916B
CR12	DIODE	SILICO			1N916B		81349	1N916B
CR13	DIODE	SILICO			1N916B		81349	1N916B

Table 7-5. DMM Motherboard, PCB Assembly 401650 (Continued)

REF DES	DESCRIPTION			FSC	MANU P/N
CR14	DIODE	POWER	3 AMP	04713	MR501
CR15	DIODE	POWER	3 AMP	04713	MR501
CR16	IC	DIODE BRIDGE	VM48	27777	VM48
CR17	DIODE	SILICO	1N916B	81349	1N916B
CR18	DIODE	SILICO		81349	1N4004
CR19	DIODE	SILICO		81349	1N4004
CR20	IC	DIODE BRIDGE	VM48	27777	VM48
CR21	DIODE			50434	HP5082-2800
CR22	DIODE	SILICO	1N916B	81349	1N916B
CR23	DIODE	SILICO	1N916B	81349	1N916B
CR24	DIODE	SILICO	1N916B	81349	1N916B
CR25	DIODE	SILICO	1N1916	81349	1N916B
J1	CONN	3 P		00779	4-583486-8
J2	CONN	7 P		00779	4-583486-4
J4	CONN	6 P		27264	09-03-1062
J201	RECEPT	24 POS		00779	552791-1
K1	RELAY	CRADLE 4 FORM C		26806	AZ421-08-204
K2	RELAY	REED 1 FORM A		71707	CR-4573
K3	RELAY	REED 1 FORM A		71707	CR4573
K4	RELAY	REED 1 FORM A		71707	CR-4573
K5	RELAY	REED 1 FORM A		71707	CR-4573
K6	RELAY	REED 1 FORM A		71707	CR-4573
K7	RELAY	REED 1 FORM A		71707	CR-4573
K8	RELAY	REED 1 FORM A		71707	CR-4573
K9	RELAY	REED 2 FORM C		26806	AZ420-08-205
K10	RELAY	REED 1 FORM A		21317	1A12R960DIAA
K11	RELAY	CRADLE 2 FORM C		26806	AZ420-08-205
K12	RELAY	CRADLE 2 FORM C		26806	AZ420-08-205
K13	RELAY	CRADLE 4 FORM C		26806	AZ421-08-204
OCI1	IC	QUAD OPTO-ISOLATOR		50579	ISO-L1TQ74
OCI2	IC	QUAD OPTO-ISOLATOR		50579	ISO-L1TQ74
OC13	IC	QUAD OPTO-ISOLATOR		50579	ISO-L1TQ74
P4	PCB ASSY	LINE VOLTAGE SELECTOR		21793	410727
Q1	TRANS	FET		27014	FM1302
Q2	TRANS	NPN		21793	200200
Q3	TRANS	NPN		21793	200200
Q4	TRANS	NPN		21793	200200
Q5	TRANS	NPN		21793	200200
Q6	TRANS	PNP		80131	2N4250
Q7	TRANS	NPN		21793	200200
Q8	TRANS	NPN	400 V	50857	DTN9000
Q9	TRANS	FET	N-CHAN, SIL JUNCTION		E305
Q10	TRANS	FET	P-CHANNEL 2N5463	04713	2N5463
Q11	TRANS	NPN		21793	200200

Table 7-5. DMM Motherboard, PCB Assembly 401650 (Continued)

REF DES	DESCRIPTION					FSC	MANU P/N
Q12	TRANS	PNP	HIGH VOLTAGE			04713	MPS-A92
Q13	TRANS	PNP				80131	2N4250
Q15	TRANS	FET	P-CHANNEL		2N5463	04713	2N5463
Q16	TRANS	FET	P-CHANNEL		2N5463	04713	2N5463
Q17	TRANS	FET	P-CHANNEL		2N5463	04713	2N5463
Q18	TRANS	NPN				21793	200200
Q19	TRANS	NPN				21793	200200
Q20	TRANS	SILICO NPN				04713	MPS-A42
Q21	TRANS	FET			2N5951	01295	2N5951
Q22	TRANS	NPN				21793	200200
Q23	TRANS	POWER				01295	TIP30
R1	POT	CERMET	50 OHM		20%	73138	89PR50
R2	RES	METAL	36.5 K		1% 1/10W	81349	RN55E3652F
R3	RES	CARBON	100 K		2% 1W	9167	SBF100K2%
R4	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R5	RES	CARBON	3 K		5% 1/4W	81349	RC07GF305J
R6	RES	METAL	40.2 K		.1% 1/10W	81349	RN55E4022B
R7	RES	METAL	40.2 K		.1% 1/10W	81349	RN55E4022B
R8	RES	METAL	4.99 K		1% 1/10W	81349	RN55C4991F
R9	RES	SET 100K/117 K		MF	0.1%	03888	A3DR24
R10	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R11	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R13	RES	CARBON	240 OHM		5% 1/4W	81349	RC07GF241J
R14	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R15	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R16	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R17	RES	CARBON	2 M		5% 1/4W	81349	RC07GF205J
R18	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R19	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R20	RES	METAL	75 K		1% 1/10W	81349	RN55C7502F
R21	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R22	RES	SET 100K/117 K		MF	0.1%	03888	A3DR24
R23	RES	CARBON	22 K		5% 1/4W	81349	RC07GF223J
R24	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R25	RES, METAL FILM		90 K OHM		1% 1.0W	03888	PME70T-9
R26	RES	CARBON	47 K		5% 2W	01121	See Description
R27	RES, METAL FILM		900 K OHM		1% .25W	03888	PME60T-9
R28	RES	METAL	9 K		.1% 1/10W	81349	RN55E9001B
R29	RES, METAL FILM		1 K OHM		1% .25W	03888	PME60T-9
R30	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R31	RES, METAL FILM		6.98 K OHM		1% .12W	03888	PME55T-9
R32	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R33	RES, METAL FILM		9 M OHM		1% 1.0W	03888	PME70T-9
R34	RES	METAL	4.42 K		1% 1/10W	81349	RN55C4421F
R35	RES, METAL FILM		787 OHM		1% .50W	03888	PME65T-9
R37	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R38	RES	CARBON	3.6 K		5% 1/4W	81349	RC07GF362J
R39	RES	CARBON	180 K		5% 1/4W	81349	RC07GF184J

Table 7-5. DMM Motherboard, PCB Assembly 401650 (Continued)

REF DES	DESCRIPTION					FSC	MANU P/N
R40	RES	CARBON	75 K		5% 1/4W	81349	RC07GF753J
R41	RES	METAL	1 K		1% 1/10W	81349	RN55D1001F
R42	RES	CARBON	390 OHM		5% 1/2W	81349	RC20GF391J
R43	RES	CARBON	390 OHM		5% 1/2W	81349	RC20GF391J
R44	RES	METAL	100 K		1% 1/10W	81349	RN55C1003F
R45	RES	METAL	49.9 K		1% 1/10W	81349	RN55C4992F
R46	RES	SET 9.9M/100 K			0.1%	03888	A3DR25
R47	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R48	RES	WW	100 K		1% 10W	21551	M-100
R49	RES	CARBON	180 OHM		5% 1/4W	81349	RC07GF181J
R50	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R51	RES	SET 9.9M/100 K		MF	0.1%	03888	A3DR25
R52	RES	CARBON	20 K		5% 2W	01121	See Description
R53	POT	CERMET	100 K			73138	68WR100K
R54	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R55	RES	METAL	909 OHM		1% 1/10W	81349	RN55C9090F
R56	RES	SET 100/900/9K		MF	0.1%	03888	A3DR23
R57	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R58	RES	CARBON	10 K		5% 1/2W	81349	RC20GF103J
R59	RES	CARBON	100 M		5% 1/4W	81349	RC07GF107J
R60	RES	METAL	49.9 K		1% 1/10W	81349	RN55C4992F
R61	RES	CARBON	100 M		5% 1/4W	81349	RC07GF107J
R62	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R63	RES	METAL	100 OHM	T-0	1% 1/8W	81349	RN60D1000F
R64	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R65	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R66	RES	METAL	1 K		1% 1/10W	81349	RN55D1001F
R67	RES	SET 100/900/9K		MF	0.1%	03888	A3DR23
R68	RES	SET 100/900/9K		MF	0.1%	03888	A3DR23
R69	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R70	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R71	RES	CARBON	10 K		5% 1/2W	81349	RC20GF103J
R72	RES	METAL	10 K		1% 1/10W	81349	RN55C1002F
R73	RES	METAL	1 K		1% 1/10W	81349	RN55D1001F
R74	RES	METAL	49.9 K		1% 1/10W	81349	RN55C4992F
R75	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R76	RES	CARBON	47 K		5% 1/4W	81349	RC07GF473J
R77	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R79	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R80	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R81	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R82	RES	CARBON	680 OHM		5% 1/2W	81349	RC20GF681J
R91	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R92	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
S1	SWITCH, SLIDE PUSHBUTTON, MOMENTARY, DPST					71590	PBI Series
S201	SWITCH		6 SPST			11237	206-6
T1	TRANS	POWER					CMI-2570

Table 7-5. DMM Motherboard, PCB Assembly 401650 (Continued)

REF DES	DESCRIPTION	FSC	MANU P/N
TP1	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP2	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP3	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP4	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP5	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP6	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP7	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP8	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP9	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP10	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP11	POST, MACHINE APPLIED STRIP	00779	1-87022-0
U1	IC	27014	DM74LS174N
U2	IC 14 DIP, DUAL D FLIP-FLOP	01295	SN74LS74N
U3	IC TRANSISTOR ARRAY	02735	CA3096E
U5	IC 14 DIP, INVERTER	01295	SN74LS05N
U6	IC 14 DIP, NAND GATE	01295	SN74LS00N
U7	IC	01295	74LS14
U8	IC 14 DIP, DUAL D FLIP-FLOP	01295	SN74LS74N
U9	IC HEX INVERTER	02735	CD4049BE
U10	IC CUSTOM SPEC.	21793	230419
U11	IC SELECTED LD120CJ	21793	230491
U12	IC LED DRIVER ICM7218A	32293	ICM7218A
U13	IC IC	01295	74LS367
U14	IC	27014	74LS138
U15	IC	27014	74LS138
U16	IC	01295	74LS367
U17	IC HEX INVERTER	02735	CD4049BE
U18	IC RELAY DRIVER MC1416P	04713	MC1416P
U19	IC RELAY DRIVER MC1416P	04713	MC1416P
U20	IC	01295	74LS367
U21	IC 14 DIP, HEX INVERTER	01295	SN74LS04N
U23	IC 14 DIP, HEX INVERTER	01295	SN74LS04N
U24	IC 14 DIP, NAND GATE	01295	SN74LS00N
U25	IC CMOS QUAD NAND GATE	02735	CD4011AE
U26	IC ANALOG SWITCHES	01295	TL601CP
U27	IC SELECTED 2716	21793	230499
U28	IC SELECTED 2716	21793	230500
U29	IC SELECTED 2716	21793	230501
U30	IC SELECTED 2716	21793	230502
U31	IC STATIC RAM MEMORY CHIP	50088	MK4118-4
U32	IC	27014	74LS175
U33	IC	02735	CD4094BE
U34	IC	02735	CD4094BE
U35	IC	04713	6802-P
U36	IC 5 CHANNEL DRIVER	56289	UHP-490
U37	IC	27014	74LS30N
U38	IC QUAD, 2 INPUT NOR GATES	01295	SN74LS02
U39	IC POSITIVE NAND GATE	01295	SN74LS10N

Table 7-5. DMM Motherboard, PCB Assembly 401650 (Continued)

REF DES	DESCRIPTION	FSC	MANU P/N
U40	IC 14 DIP, DUAL D FLIP-FLOP	01295	SN74LS74N
U41	IC MOS BILATERAL SWITCH	18722	CD4066AD
U42	IC CMOS QUAD NAND GATE	02735	CD4011AE
U43	IC CMOS MEMORY	32293	IM6508
U44	IC	04713	MC68488L
U45	IC	01295	74LS367
U46	IC BUFFER	04713	MC3447P3
U47	IC BUFFER	04713	MC3447P3
U48	IC	04713	MC7812-CT
U49	IC	27014	7915CT
U50	IC 5.0 V	04713	MC7805CT
U51	IC 5.0 V	04713	MC7805CT
U52	IC +8 VOLT REGULATOR	04713	MC7808CT
VR1	IC (+7V REFERENCE)	27014	LM399H
VR2	IC +7V REFERENCE	27014	LM3999Z
VR3	DIODE ZENER 30 V	04713	1N972B
VR4	DIODE SILICO, ZENER	81349	1N4370
VR5	DIODE ZENER	82349	1N753A
VR6	DIODE ZENER 16 V 5%	81349	1N966B
VR7	DIODE SILICO, ZENER	81349	1N751A
VR8	DIODE ZENER 24 V 5%	81349	1N970B
VR9	DIODE ZENER 24 V 5%	81349	1N970B
VR10	DIODE ZENER	81349	1N753A
VR11	DIODE ZENER	81349	1N753A
VR12	DIODE ZENER 5.1 V	01281	LVA51A
VR13	DIODE ZENER 30 V	04713	1N972B
VR14	DIODE ZENER 30 V	04713	1N972B
VR15	DIODE SILICO, ZENER	81349	1N967B
VR16	DIODE SILICO, ZENER	81349	1N967B
W1	JUMPER, INSULATED		L-2007-1LP
Y1	CRYSTAL 2.4576 MHz		2.4576 MHz
Y2	CRYSTAL 3.579 MHz		1107863-1
Z1	RES CERMET 1 K Network 8P,7R 2%	11236	750-81-R1K
Z2	RES CERMET 10 K Network 8P,7R 2%	11236	750-81-R10K
Z3	RES CERMET 22 K Network 8P,7R 2%	11236	750-81-R22K
Z4	RES CERMET 1 K Network 8P,7R 2%	11236	750-81-R1K
Z5	RES CERMET 10 K Network 8P,7R 2%	11236	750-81-R10K
Z6	RES CERMET 500 OHM Network 8P,7R 2%	11236	750-81-R500
Z7	RES CERMET 22 K Network 8P,7R 2%	11236	750-81-R22K
Z8	RES CERMET 10 K Network 8P,7R 2%	11236	750-81-R10K
Z9	RES CERMET 10 K Network 8P,7R 2%	11236	750-81-R10K
Z10	RES CERMET 10 K Network 8P,7R 2%	11236	750-81-R10K

Table 7-6. DMM AC Converter, PCB Assembly 404107

REF DES	DESCRIPTION						FSC	MANU P/N
B1	BEAD	SHIELDING			56-59065/4B		02114	56-59065/4B
B2	BEAD	SHIELDING			56-59065/4B		02114	56-59065/4B
B3	BEAD	SHIELDING			56-59065/4B		02114	56-59065/4B
C1	CAP	MYLAR	.22	MFD	1000 V	10%	27556	ZA1J224K
C2	CAP	TRIMMER	.25-1.5	PFD			74970	273-0001-002
C3	CAP	ELECT	100	MFD	25 V		34553	ET101X025A5
C4	CAP	CERAM	.01	MFD	100 V		71471	Type TTP
C5	CAP	CERAM	.01	MFD	100 V		71471	Type TTP
C6	CAP	TANTA	2.2	MFD	35 V	10%	05397	T310B225K035AS
C7	CAP	ELECT	100	MFD	25 V		34553	ET101X025A5
C8	CAP	TANTA	68	MFD	6 V	20%	05397	T368B686M006AS
C9	CAP	CERAM	200	PFD	1000 V	20%	71471	GPDX5F201K
C10	CAP	TANTA	1	MFD	35 V	20%	05397	T368A105M035AS
C12	CAP	CERAM	200	PFD	1000 V	20%	71471	GPDX5F201K
C13	CAP	MYLAR	1.5	MFD	100 V	20%	73445	C281AH/A1M5
C14	CAP	MYLAR	1.5	MFD	100 V	20%	73445	C281AH/A1M5
C16	CAP	MYLAR	1.5	MFD	100 V	20%	73445	C281AH/A1M5
C17	CAP	MYLAR	1.5	MFD	100 V	20%	73445	C281AH/A1M5
C18	CAP	MYLAR	.22	MFD	100 V	20%	73445	C281AH/A220K
C19	CAP	MYLAR	.22	MFD	100 V	20%	73445	C281AH/A220K
C20	CAP	CERAM	.05	MFD	100 V	20%	56289	C023A101L503M
C21	CAP	CERAM	.02	MFD	100 V	20%	56289	C023B101H203M
C22	CAP	CERAM	.01	MFD	100 V		71471	Type TTP
C23	CAP	ELECT	22	MFD	25 V		34553	ET220X025A3
C24	CAP	CERAM	.01	MFD	100 V		71471	Type TTP
C25	CAP	ELECT	22	MFD	25 V		34553	ET220X025A3
C26	CAP	TRIMMER	.25-1.5	PFD			74970	273-0001-002
C27	CAP	CERAM	5.6	PFD	1000 V	5%	56289	C023B102E5R6D
C28	CAP	CERAM	2.2	PFD	1000 V	5%	56289	C030B102S2R2D
C29	CAP	TRIMMER	1.2-10	PFD	250 V		52763	R-TRIKO-122-09SD
C30	CAP	CERAM	FSV		100100		21793	100100
C31	CAP	POLY	47	PFD	125 V	10%	26625	611
C32	CAP	ELECT	22	MFD	25 V		34553	ET220X025A3
C33	CAP	CERAM	FSV		100100		21793	100100
C34	CAP	TRIMMER	5-20	PFD	250 V		52763	R-TRIKO-122-09MG
C35	CAP	POLY	680	PFD	630 V	5%	08257	KSO Series
C36	CAP	CERAM	100	PFD	500 V	10%	04222	TCD-DI-1N5600-100
C37	CAP	POLY	.015	MFD	33 V	10%	26625	611.3S
C38	CAP	CERAM	.01	MFD	100 V		71471	Type TTP
CR1	DIODE				HP5082-2800		50434	HP5082-2800
CR2	DIODE				HP5082-2800		50434	HP5082-2800
CR3	DIODE				HP5082-2800		50434	HP5082-2800
CR4	DIODE				HP5082-2800		50434	HP5082-2800
CR5	DIODE	SILICO					81349	1N916B
CR6	DIODE	SILICO					81349	1N916B
CR7	DIODE	SILICO					81349	1N916B
CR8	DIODE	SILICO	ZENER				81349	1N965B

Table 7-6. DMM AC Converter, PCB Assembly 404107 (Continued)

REF DES	DESCRIPTION				FSC	MANU P/N
CR9	DIODE	SILICO	ZENER		81349	1N965B
CR10	DIODE	SILICO	ZENER		81349	1N965B
CR11	DIODE	SILICO			81349	1N916B
K1	RELAY	REED		R2699-2	15636	R2699-2
K2	RELAY	REED		R2699-2	15636	R2699-2
K3	RELAY	REED		R2699-2	15636	R2699-2
Q1	TRANS		FET	2N4302	80131	2N4302
Q2	TRANS	SILICO	NPN	EN916	07263	EN916
Q3	TRANS	DUAL	NPN	200201	21793	200201
Q4	TRANS		PNP	2N4917	81349	2N4917
Q5	TRANS		PNP	2N4917	81349	2N4917
Q6	TRANS		PNP	2N4917	81349	2N4917
Q7	TRANS		PNP	2N4917	81349	2N4917
Q8	TRANS	SILICO	NPN	EN916	07263	EN916
R1	RES	METAL		MATCHED SET	21793	010794
R2	RES	CARBON	FSV	5% 1/4W	21793	001737
R3	RES	CARBON	36 K	5% 1/4W	81349	RC07GF363J
R4	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R5	RES	CARBON	4.7 K	5% 1/4W	81349	RC07GF472J
R6	RES	CARBON	36 K	5% 1/4W	81349	RC07GF363J
R7	RES	CARBON	43 K	5% 1/4W	81349	RC07GF433J
R8	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R9	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R10	RES	CARBON	360 OHM	5% 1/4W	81349	RC07GF361J
R11	RES	CARBON	27 OHM	5% 1/4W	81349	RC07GF270J
R12	RES	CARBON	3.6 K	5% 1/4W	81349	RC07GF362J
R13	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R14	RES	CARBON	22 K	5% 1/4W	81349	RC07GF223J
R15	RES	CARBON	2.4 M	5% 1/4W	81349	RC07GF245J
R16	RES	CARBON	360 OHM	5% 1/4W	81349	RC07GF361J
R17	RES	CARBON	5.6 K	5% 1/4W	81349	RC07GF562J
R18	RES	CARBON	43 K	5% 1/4W	81349	RC07GF433J
R19	POT	CERMET	100 K	10%	73138	89PR100K
R20	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R21	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R22	RES	CARBON	27 OHM	5% 1/4W	81349	RC07GF270J
R23	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R24	RES	CARBON	330 OHM	5% 1/4W	81349	RC07GF331J
R28	RES	METAL		MATCHED SET	21793	010793
R29	RES	METAL		MATCHED SET	21793	010793
R30	RES	METAL		MATCHED SET	21793	010793
R31	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R32	RES	CARBON	5.6 K	5% 1/4W	81349	RC07GF562J
R33	RES	METAL	40 K	Pair with R34	21793	010744
R34	RES	METAL	40 K	Pair with R33	21793	010744
R35	RES	METAL	40 K	Pair with R36	21793	010744

Table 7-6. DMM AC Converter, PCB Assembly 404107 (Continued)

REF DES	DESCRIPTION						FSC	MANU P/N
R36	RES	METAL	40 K	Pair with R35			21793	010744
R37	RES	METAL	20 K	Pair with R38			21793	010743
R38	RES	METAL	20 K	Pair with R37			21793	010743
R39	RES	METAL	200 K	Pair with R40	.1%		21793	010792
R40	RES	METAL	200 K	Pair with R39	.1%		21793	010792
R41	POT	CERMET	20 K		10%		73138	89PR20K
R42	RES	CARBON	10 OHM		5%	1/4W	81349	RC07GF100J
R43	RES	CARBON	39 OHM		5%	1/4W	81349	RC07GF390J
R44	POT	CERMET	1 K		10%		73138	89PR1K
R45	RES	METAL	71.5 K		1%	1/10W	81349	RN55C7152F
R46	RES	METAL		MATCHED SET			21793	010794
R47	POT	CERMET	1 K		10%		73138	89PR1K
R48	RES	METAL		MATCHED SET			21793	010794
R49	POT	CERMET	100 OHM		10%		73138	89PR100
R50	RES	METAL		MATCHED SET			21793	010794
R51	POT	CERMET	2 K		10%		73138	89PR2K
R52	RES	METAL	13.7 K		1%	1/10W	81349	RN55C1372F
R53	JUMPER			L-2007-1LP				L-2007-1LP
R54	RES	METAL		MATCHED SET			21793	010794
R55	RES	CARBON	FSV	001737	5%	1/4W	21793	001737
U1	INTEGRATED CIRCUIT			SSS725C			06665	SSS725C

Table 7-7. Digital Multimeter Mod Assembly 3102494-003

ITEM	REF DES	DESCRIPTION	FSC CODE	PART NUMBER	QTY
1	M1	DIGITAL MULTIMETER	21793	5005-S-4622	1
2	N/A	CHASSIS ASSY	12436	3102502-005	1
3	N/A	COVER	12436	3102505-002	1
4	PS1	POWER SUPPLY	53279	XM-15-5	1
5	CB1	SWITCH	81541	T11-1-1.00A-01-10AL	1
6	A1	CKT CARD ASSY	12436	3102498-003	1
7	S1	SWITCH	12436	6011184-001	1
8	J5	RECEPTACLE	19048	160-2-N	1
9	FL1	FILTER	05245	1VK1	1
10	S2	SWITCH	09353	7213J61ZQ	1
11	N/A	IDEN PLATE	58189	A29907-002	1
12	W1	CABLE ASSY	12436	3102519-001	1
13	N/A	SCREW	96906	MS24693C48	8
14	N/A				
15	FF-M-836	NUT	96906	MS35650-304	1
16					
17					
18	FF-S-92	SCREW, PAN HD	96906	MS24693C270	4
19		SCREW	96906	MS51958-60	1
20	FF-W-84	WASHER, LOCK	96906	MS35338-138	2
21	FF-W-92	WASHER, FLAT	96906	MS15795-803	22
22	FF-W-84	WASHER, LOCK	96906	MS35338-135	22
23	FF-N-836	NUT	96906	MS35649-244	22
24	FF-S-92	SCREW, PAN HD	96906	MS51957-16	14
25	N/A	SCREW	96906	MS51959-15	8
26	N/A	SPACER	80205	NAS43DD1-64	2
27	FF-W-84	WASHER, LOCK	96906	MS35338-136	9
28	FF-N-836	NUT	96906	MS35649-264	2
29	N/A	SCREW	96906	MS51957-36	2
30	FF-W-92	WASHER, FLAT	96906	MS15795-805	9
31	FF-S-92	SCREW	96906	MS51957-27	7
32	FF-S-92	SCREW	96906	MS51958-63	2
33	N/A	SCREW	96906	MS51957-8	2
34	FF-W-92	WASHER, FLAT	96906	MS15795-802	2
35	N/A				
36	N/A				
37	N/A	SIGN DANGER	12436	2117943-001	1
38	N/A	PLATE	12436	2117943-002	1
39	N/A	CLAMP	59730	TC105A	10
40	N/A	SOLVENT	59730	TC110	1 OZ
41	N/A	STRAP, CABLE	96906	MS3367-1-9	10
42	MIL-S-22473	COMPOUND, SEALING	81349	GRADE E	.010 OZ
43	N/A				
44					
45	N/A	PLATE	12436	3102540-001	1
46	N/A	PLATE, MOUNTING	12436	3102541-004	2
47	FF-W-92	WASHER, FLAT	88044	AN960C8L	12
48	FF-W-92	WASHER, FLAT	88044	AN960C8	8
49	FF-S-92	WASHER, FLAT	96906	MS15795-807	8
50	FF-S-92	SCREW	96906	MS24693C50	8

Table 7-7. Digital Multimeter Mod Assembly 3102494-003 (Continued)

ITEM	REF DES	DESCRIPTION	FSC CODE	PART NUMBER	QTY
51	N/A	PLATE, GROUND	12436	3102549-001	1
52	N/A	LABEL	12436	3102568-101	1
53	J1, J6	CONNECTOR	96906	MS3122E12-8P	2
54	J2	CONNECTOR	96906	MS3122E12-3P	1
55	J3	CONNECTOR	96906	MS3122E20-41PW	1
56	J4	CONNECTOR	96906	MS3122E20-41P	1
57	P1, P3	PLUG	83330	212-101	2
58	P2, P4	PLUG	83330	212-103	2
59	P5	PLUG	83330	212-104	1
60	N/A	WIRE WRAP	12436	3104294-901	1

Table 7-8. Interface Circuit Card Assembly 3102498

ITEM	REF DES	DESCRIPTION	FSC CODE	PART NUMBER	QTY
1	N/A				
2	N/A	PWB	12436	3102500-001	1
3	N/A				
4	C1-9, 11,12, 15-19, 21-23 25-30, 32-35	CAPACITOR	81349	CKR06BX103KS	29
5	U1-2, 10-13, 20-22, 26-29, 35-37, 41, 42, 49, 58	IC	54893	HCPL-2730	
6	U47, 48, 53, 54	IC	84713	MC3441AP	4
7	U9, 25	IC	23223	760-1-R1K	2
8	U19, 34	RESISTOR	73138	899-1-R4.7K	2
9	U8, 18, 33, 40	IC	01295	74LS253N	4
10	U7	IC	34649	ID8212	1
11	Y1	CRYSTAL	23223	MP05A	1
12	U32	IC	34649	ID8085AH	1
13	U46	IC	34649	ID8155H	1
14	S1	SWITCH	81073	39-251BLK	1
15	CR1, 2	DIODE	81350	1N914	2
16	MIL-R-39017/1 R4	RESISTOR	81349	RLR07C47R0GM	1
17	MIL-R-39017/1 R3	RESISTOR	81349	RLR07C1003FM	1
18	MIL-C-39014/2 C10	CAPACITOR	81349	CKR06BX105KS	1
19	U6	IC	12436	6010854-003	1
20	U31, 39	IC	01295	SN74LS32N	2
21	U45	IC	01295	SN74LS04N	1
22	U4, 15, 44, 52	IC	01295	SN74LS164N	4
23	U23, 38	IC	23223	760-1-R180	2
24	U3, 14, 43, 51	IC	01295	SN7406N	4
25	MIL-R-39017/1 R8	RESISTOR	81349	RLR07C3302GM	1
26	MIL-R-39017/1 R6	RESISTOR	81349	RLR07C4301FM	1
27	MIL-R-39017/1 R7	RESISTOR	81349	RLR07C1103FM	1
28	MIL-S-19500/291 Q1	TRANSISTOR	81350	2N2907	1

Table 7-8. Interface Circuit Card Assembly 3102498

ITEM	REF DES	DESCRIPTION	FSC CODE	PART NUMBER	QTY
29	Q2	TRANSISTOR	81350	2N2222	1
30	MIL-R-39017/1 R1,5	RESISTOR	81349	RLR07C1001FM	2
31	MIL-R-39017/1 R2,9	RESISTOR	81349	RLR07C1002FM	2
32	C24, 31	CAPACITOR	56289	150D226X9006B2	2
33	J1	CONNECTOR	19048	57-40240-9	1
34	MIL-S-83734/8 XU6	SOCKET	81349	M83734/8-013	1
35	MIL-S-83734/10 XU32	SOCKET	81349	M83734/8-013	1
36	N/A	TERMINAL, W/W	71279	155-1077-01-03	59
37	U16	IC	01295	SN74LS02J	1
38	U5	IC	01295	SN74LS00J	1
39	U30	IC	07263	UA555TC	1
40	U24	IC	07263	UA556PC	1
41	MIL-C-39014/2 C20	CAPACITOR	81349	CKR06BX473KS	1
42	N/A				
43	N/A				
44	CR3-42	LED	72619	555-3001	40
45	N/A	SPACER	12436	3102514-001	2
46	MIL-I-46058	COMPOUND, INSULATING 99	81349	TYPE AR	0.1 OZ
47	MIL-S-22473	SEALANT	81349	GRADE P	0.1 OZ
48	N/A	ADHESIVE 99	12436	7010037-001	0.1 OZ
49	QQ-W-343	WIRE 99	58189	820104-072	0.5 FT
50	N/A				

Table 7-9. Interface Cable W1 Assembly 3102519

ITEM	REF DES	DESCRIPTION	FSC CODE	PART NUMBER	QTY
1	N/A	CABLE	9747	16428	20 IN.
2	P1	CONNECTOR	57-30240	02660	1
3	N/A	SLEEVING 99	Y00037-158	58189	1 FT
4	P2	CONNECTOR	552661-1	00779	1

APPENDIX A

DIGITAL MICROCIRCUIT 2K X 8
UV ERASABLE PROM

6010854-003

(Intel Corporation Part Number ID 2716)

A-1. Table 1 defines the requirements for programming the 2K X 8 UV erasable PROM.

A-2. After programming, the PROM shall be identified with part number 6010854-003.

A-3. An ultra-violet opaque tape shall be placed over the EPROM window after programming. The tape shall be Intel Corporation part number 0005000 or equivalent.

Table A-1. UV Erasable PROM Program for 6010854-003

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000000	1E	00	3E	80	30	3E	0F	D3	40	AF	D3	80	D3	80	D3	80
000010	D3	80	D3	80	C3	32	00	7A	D3	80	0F	0F	0F	0F	D3	80
000020	AF	D3	80	D3	80	D3	80	3E	F0	D3	42	3E	FF	D3	42	C3
000030	27	00	16	41	AF	4F	21	00	60	77	23	3C	0C	C2	39	00
000040	21	00	60	BE	C2	17	00	23	3C	0C	C2	43	00	47	DB	42
000050	E6	0F	D3	42	F6	F0	D3	42	78	3C	C2	36	00	31	FF	60
000060	20	17	DA	39	01	06	05	AF	D3	80	05	C2	68	00	16	00
000070	21	10	01	19	7E	D3	80	23	46	AF	05	CA	83	00	D3	80
000080	C3	7A	00	16	60	DB	83	CD	45	05	16	50	DB	82	CD	45
000090	05	3E	C0	30	3E	01	06	08	16	70	4F	AF	D3	41	DB	80
0000A0	A1	C2	17	00	14	79	D3	41	DB	80	A1	CA	17	00	07	14
0000B0	05	C2	9A	00	06	04	16	80	CD	2A	05	C2	17	00	3E	40
0000C0	30	3E	10	06	02	CD	2A	05	C2	17	00	DB	81	17	DA	17
0000D0	00	14	17	DA	17	00	16	90	3E	0D	D3	40	DB	42	CD	04
0000E0	01	3E	0F	D3	40	3E	F0	D3	42	DB	42	2F	CD	04	01	28
0000F0	7E	F6	F0	D3	42	23	23	1C	1C	3E	FF	BE	C2	32	00	1E
000100	00	C3	32	00	06	04	1F	D2	17	00	14	05	C2	06	01	C9
000110	01	05	02	05	04	05	08	05	01	04	02	04	04	04	08	04
000120	01	03	02	03	04	03	08	03	01	02	02	02	04	02	08	02
000130	01	01	02	01	04	01	08	01	FF	AF	D3	80	D3	80	D3	80
000140	D3	80	D3	80	3E	F0	D3	42	3E	00	32	08	60	31	FF	60
000150	3E	00	32	03	60	32	02	60	21	BA	03	06	03	CD	13	06
000160	DB	82	57	DB	83	5F	CD	51	05	DB	83	BB	C2	60	01	DB
000170	82	BA	C2	60	01	21	00	60	73	23	72	17	D2	86	01	17
000180	D2	86	01	C3	60	01	D5	21	BD	03	06	03	CD	13	06	D1
000190	20	32	07	60	3E	08	32	0B	60	C3	A9	01	3A	00	60	17
0001A0	17	D2	A9	01	3E	07	32	0B	60	21	03	60	72	2B	73	7A
0001B0	2F	0E	06	21	25	03	06	14	23	05	C2	B8	01	1F	DA	CA
0001C0	01	0D	C2	B6	01	16	11	C3	58	06	7B	2F	0E	05	06	04
0001D0	1F	DA	E2	01	23	05	C2	D4	01	0D	C2	CE	01	16	12	C3
0001E0	58	06	E5	06	14	11	21	03	21	10	60	1A	77	13	23	05
0001F0	C2	EB	01	E1	06	02	11	11	60	7E	12	23	13	13	05	C2
000200	F9	01	7E	32	04	60	23	7E	32	05	60	21	00	60	7E	07
000210	DA	18	02	3E	31	32	17	60	3A	13	60	FE	33	C2	5E	02
000220	3E	31	32	17	60	3E	31	32	1D	60	3A	07	60	17	D2	38
000230	02	AF	32	06	60	C3	5E	02	3A	01	60	17	D2	46	02	3A
000240	06	60	B7	C2	5E	02	06	06	11	B2	03	CD	6E	05	CD	DE
000250	06	3E	01	32	06	60	06	02	11	B8	03	CD	6E	05	21	01
000260	60	7E	E6	08	CA	6D	02	7E	E6	10	C2	73	02	3E	31	32
000270	1F	60	7E	3A	04	60	B7	F2	87	02	21	BA	03	06	03	CD
000280	13	06	16	19	C3	58	06	3A	01	60	E6	40	CA	16	03	06
000290	14	3A	01	60	E6	20	C2	A6	02	3A	11	60	32	0C	60	3E
0002A0	37	32	11	60	06	12	11	10	60	CD	6E	05	3A	0B	60	47
0002B0	21	50	60	3E	3A	77	23	05	C2	B5	02	06	14	3A	00	60
0002C0	E6	20	C2	C7	02	06	32	78	32	0A	60	3A	04	60	CD	51
0002D0	05	3A	00	60	17	DA	DE	02	3A	04	60	CD	51	05	06	02
0002E0	11	B6	03	CD	6E	05	CD	DE	06	3A	B2	00	E6	04	C2	C0
0002F0	03	0E	43	CD	51	05	0D	C2	F3	02	06	02	11	B6	03	CD

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Table A-1. UV Erasable PROM Program for 6010854-003 (Continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000300	6E	05	CD	DE	06	C3	C0	03	0E	0D	CD	51	05	0D	C2	0A
000310	03	3D	C2	08	03	C9	06	12	11	12	60	CD	6E	05	C3	DE
000320	02	52	30	46	31	54	33	4A	30	44	31	49	32	4E	30	47
000330	30	51	30	52	30	3F	20	0D	0A	33	31	12	00	33	31	12
000340	FF	30	30	F6	00	30	30	F6	00	30	30	F6	00	36	32	13
000350	03	35	32	13	02	34	32	13	01	30	30	F6	00	30	30	F6
000360	00	37	33	12	06	36	33	12	05	35	33	12	04	34	33	12
000370	03	38	33	12	07	35	31	14	02	34	31	14	01	33	31	14
000380	00	30	30	F6	00	30	30	F6	00	35	31	14	02	34	31	14
000390	01	33	31	14	00	30	30	F6	00	30	30	F6	00	37	31	12
0003A0	03	36	31	12	02	35	31	12	01	30	30	F6	00	30	30	F6
0003B0	00	5F	52	30	4E	30	54	30	4E	32	3F	20	01	3F	20	11
0003C0	21	30	60	3E	01	F5	CD	D5	05	73	23	7B	FE	0A	CA	DE
0003D0	03	F1	FE	0E	16	21	CA	58	06	3C	F5	C3	C6	03	F1	FE
0003E0	0E	16	22	C2	58	06	21	B1	03	06	01	CD	13	06	3A	3B
0003F0	60	E6	0F	4F	3A	39	60	FE	2B	CA	FF	03	AF	91	4F	79
000400	C6	40	4F	3A	01	60	E6	20	C2	1B	04	E5	21	11	60	3A
000410	05	60	86	21	0C	60	96	E1	F2	1E	04	3A	05	60	C6	40
000420	B9	CA	35	04	D2	2E	04	0D	CD	3C	06	C3	03	04	0C	CD
000430	26	06	C3	03	04	3A	3A	60	FE	30	C2	92	06	3A	31	60
000440	E6	F0	C2	92	06	3E	F0	D3	42	3A	01	60	47	2F	E6	18
000450	CA	86	04	3A	30	60	FE	2B	CA	7B	04	78	E6	08	CA	66
000460	04	3E	2D	C3	68	04	3E	2B	32	30	60	06	05	3E	09	21
000470	33	60	77	23	05	C2	72	04	C3	86	04	78	E6	08	CA	86
000480	04	3E	2D	32	30	60	3A	30	60	FE	2B	CA	92	04	3E	F1
000490	D3	42	3A	01	60	17	DA	AE	04	3A	0B	60	47	21	50	60
0004A0	11	30	60	1A	BE	C2	F2	04	23	13	05	C2	A3	04	21	37
0004B0	60	06	05	7E	D3	80	2B	05	C2	B3	04	3A	01	60	E6	40
0004C0	CA	CC	04	0E	43	CD	51	05	0D	C2	C5	04	3A	01	60	17
0004D0	DA	58	01	DB	42	47	3A	0A	60	B7	C2	E1	04	78	F6	04
0004E0	47	78	F6	02	D3	42	CD	51	05	DB	42	E6	F1	D3	42	C3
0004F0	58	01	3A	0A	60	3D	32	0A	60	CA	AE	04	06	08	21	50
000500	60	11	30	60	1A	77	23	13	05	C2	04	05	3A	01	60	E6
000510	20	C2	DE	02	21	11	60	3A	0C	60	BE	CA	1F	05	35	11
000520	10	60	06	02	CD	6E	05	C3	DE	02	4F	AF	D3	43	DB	81
000530	A1	C2	17	00	14	79	D3	43	DB	81	A1	CA	17	00	07	14
000540	05	C2	2A	05	C9	06	08	1F	D2	17	00	14	05	C2	47	05
000550	C9	06	FF	C5	C1	05	C2	53	05	47	DB	42	E6	0F	D3	42
000560	F6	F0	D3	42	78	C9	06	02	00	05	C8	C3	68	05	3E	0A
000570	D3	43	3E	C0	30	21	35	03	CD	96	05	23	CD	96	05	3E
000580	08	D3	43	EB	CD	96	05	23	05	C2	84	05	EB	23	CD	96
000590	05	23	CD	96	05	C9	DB	81	E6	FE	D3	43	7E	D3	41	0E
0005A0	FF	DB	81	07	07	07	D2	C9	05	2F	E6	80	C2	B8	05	0D
0005B0	C2	A1	05	16	33	C3	58	06	0E	FF	DB	81	F6	01	D3	43
0005C0	E6	20	CA	CE	05	0D	C2	BA	05	16	34	C3	58	06	DB	81
0005D0	E6	FE	D3	43	C9	DB	81	F6	30	D3	43	CD	66	05	E6	EF
0005E0	D3	43	0E	FF	DB	81	0F	DA	F3	05	0D	C2	E4	05	16	35
0005F0	C3	58	06	DB	81	F6	10	D3	43	DB	80	5F	0F	FF	DB	81

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Table A-1. UV Erasable PROM Program for 6010854-003 (Continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000600	E6	DF	D3	43	E6	20	CA	12	06	0D	C2	FE	05	16	36	C3
000610	58	06	C9	3E	0A	D3	43	3E	C0	30	CD	96	05	23	05	C2
000620	1A	06	3E	40	30	C9	21	37	60	11	36	60	06	04	1A	77
000630	1B	2B	05	C2	2E	06	18	1A	77	AF	12	C9	21	33	60	11
000640	31	60	1A	E6	30	C2	92	06	7E	12	13	06	04	13	23	7E
000650	12	05	C2	4D	06	AF	77	C9	D5	7A	D3	80	0F	0F	0F	0F
000660	D3	80	AF	D3	80	D3	80	D3	80	3E	F6	16	6C	CD	51	05
000670	15	C2	6D	06	D3	42	16	03	CD	51	05	15	C2	78	06	3E
000680	F0	D3	42	F1	FE	11	CA	48	01	DB	82	07	DA	83	06	C3
000690	48	01	3E	09	06	05	D3	80	05	C2	96	06	CD	CA	06	0E
0006A0	1A	CD	51	05	0D	C2	A1	06	CD	CA	06	3A	01	60	07	DA
0006B0	4D	01	DB	42	F6	02	D3	42	0E	02	CD	51	05	0D	C2	BA
0006C0	06	DB	42	E6	F1	D3	42	C3	4D	01	DB	42	F6	08	D3	42
0006D0	0E	0D	CD	51	05	0D	C2	D2	06	E6	F1	D3	42	C9	3E	40
0006E0	30	0E	FF	DB	81	E6	40	C2	FC	06	3E	0A	CD	51	05	3D
0006F0	C2	EC	06	0D	C2	E3	06	16	38	C3	58	06	21	18	07	06
000700	04	CD	13	06	CD	D5	05	06	01	CD	13	06	3E	40	30	3E
000710	41	88	C8	16	37	C3	58	06	5F	3F	18	40	19	77	23	13
000720	05	C2	15	07	36	20	23	36	20	23	13	13	1A	CD	AB	12
000730	1B	1A	CD	AB	12	36	0D	23	36	00	13	13	13	13	D5	21
000740	5E	18	CD	ED	10	D1	1A	FE	00	C2	10	07	C9	2A	90	1A
000750	22	80	1A	22	82	1A	36	80	3A	65	1A	32	66	1A	21	13
000760	2C	22	92	1A	CD	C2	13	2A	92	1A	CD	74	06	CD	AE	11
000770	21	22	18	CD	02	22	B7	C2	AE	0C	21	97	1A	7E	32	74
000780	1A	23	23	7E	23	22	8A	1A	E6	0F	FE	02	C2	C9	0C	3A
000790	74	1A	B7	CA	E0	07	2A	8A	1A	22	7E	1A	11	08	00	19
0007A0	7E	E5	CD	D6	09	E1	E6	20	C2	BE	07	23	CD	06	0A	21
0007B0	84	1A	72	23	73	CD	9D	0D	79	E6	01	C4	26	0D	2A	8A
0007C0	1A	11	0B	00	19	22	8A	1A	3A	74	1A	D6	0B	32	74	1A
0007D0	DA	D9	0C	C2	96	07	3A	99	1A	07	D2	70	07	CD	40	12
0007E0	2A	92	1A	CD	48	06	2A	92	1A	11	7A	00	19	22	92	1A
0007F0	3A	66	1A	3D	32	66	1A	C2	67	07	C9	3A	65	1A	32	66

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